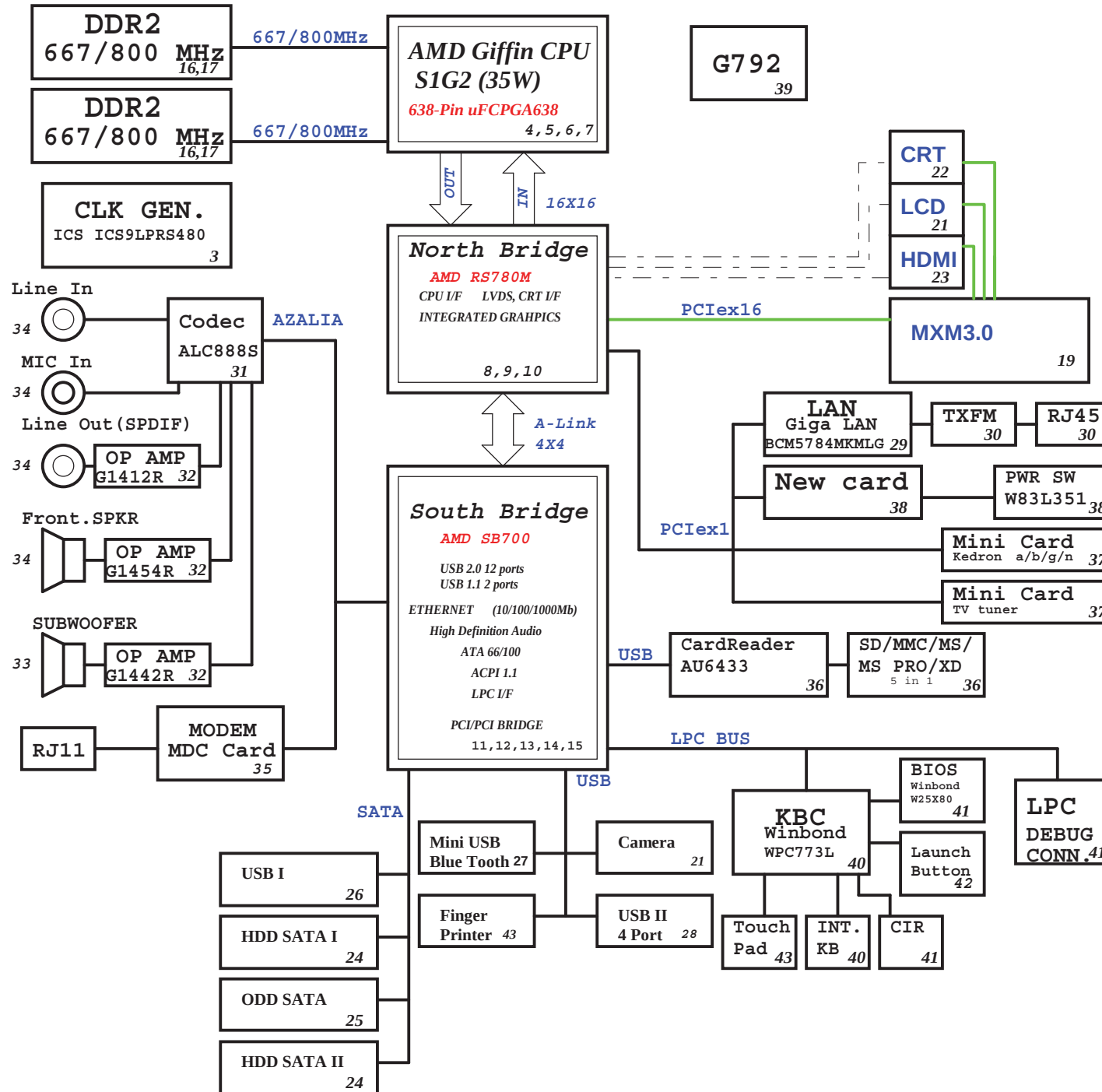


JM70-PU (AS 17") Block Diagram

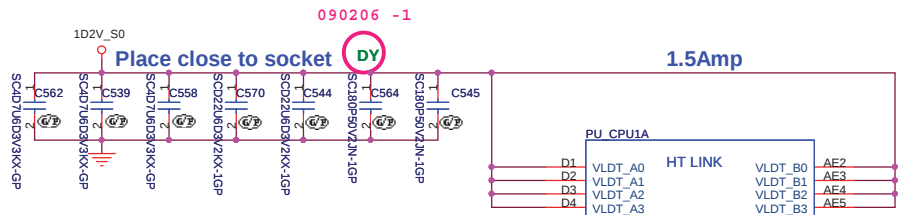
Project code: 91.4CE01.001
PCB P/N : 48.4CE01.0SC
REVISION : 08255-SC



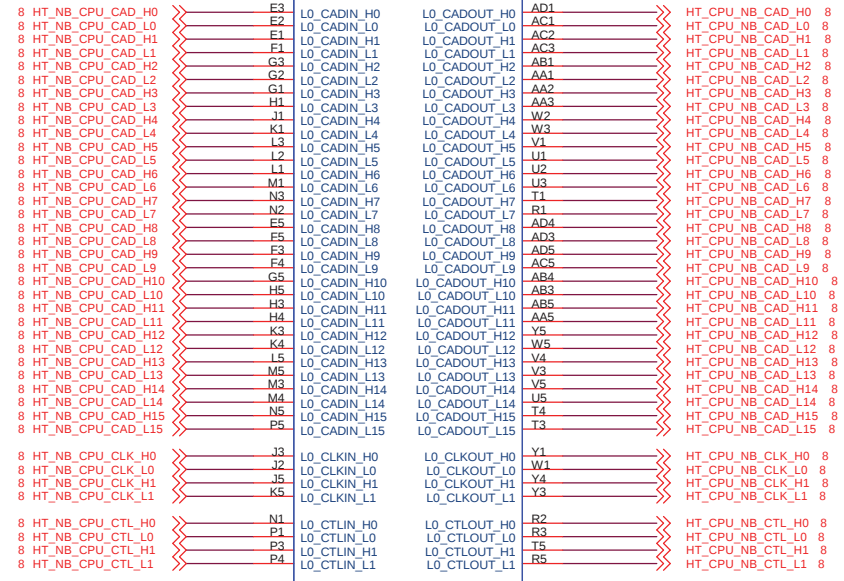
PCB STACKUP
TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51125 49	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (7A)
	3D3V_S5 (7A)
SYSTEM DC/DC TPS51124 50	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0 (8A)
	1D2V_S0 (5A)
SYSTEM DC/DC TPS51117 52	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 (10A)
RT9026PFP 51	
1D8V_S3	DDR_VREF_S3
	0D9V_S3 (1A)
RT9166 51	
3D3V_S0	2D5V_S0 (300mA)
G957 51	
3D3V_S0	1D5V_S0 (1A)
G9161 (UMA) 51	
3D3V_S5	1D2V_S5 (400mA)
G9131 (DIS) 51	
3D3V_S5	1D2V_S5 (300mA)
CHARGER MAX8731A 53	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR
	18V 6.0A
	UP+5V
	5V 100mA
CPU DC/DC ISL6265HR 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0
	0~1.55V 18A
	VCC_CORE_S0_1
	0~1.55V 18A
	VDDNB
	0~1.55V 18A

<Core Design>



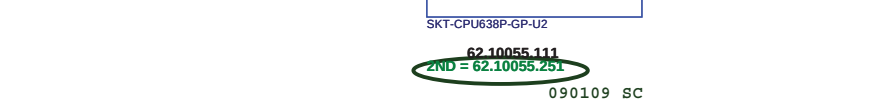
State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V



SKT-CPU638P-GP-U2

62 10055 111
ZND = 62.10055.251

090109 SC
SKT-BGA638H176



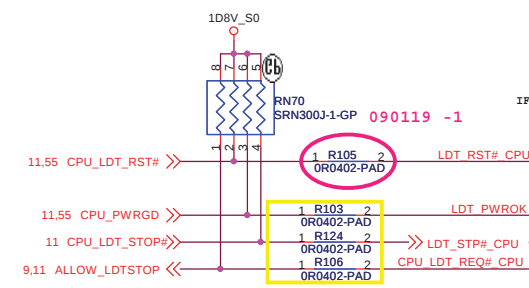
SKT-CPU638P-GP-U2

62.10055.111 090109 SC
2ND = 62.10055.251

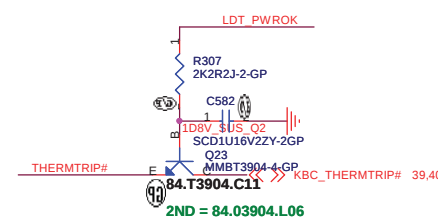
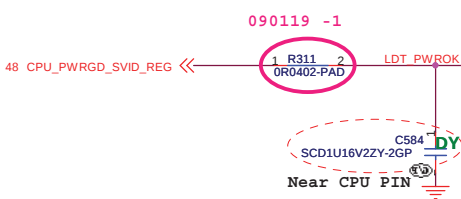
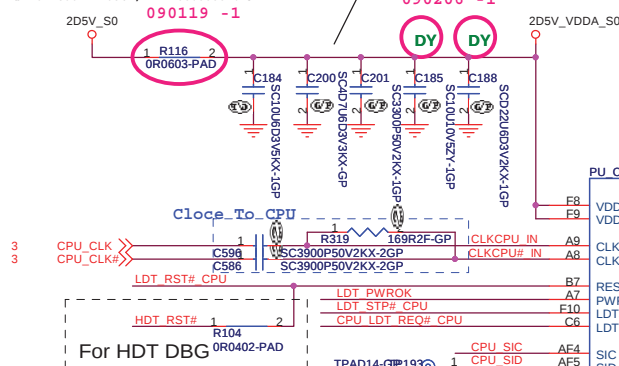
Care Design>

LYAOUT:ROUTE VDDA TRACE APPROX.
40 mils WIDE
(USE 2X25 mil TRACES TO EXIT BALL FIELD)
& 500 mils LONG.

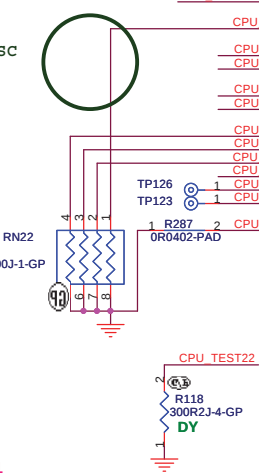
The Processor has
reached a preset
maximum operating
temperature. 100°C
I=Active HTC
O=FAN



IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

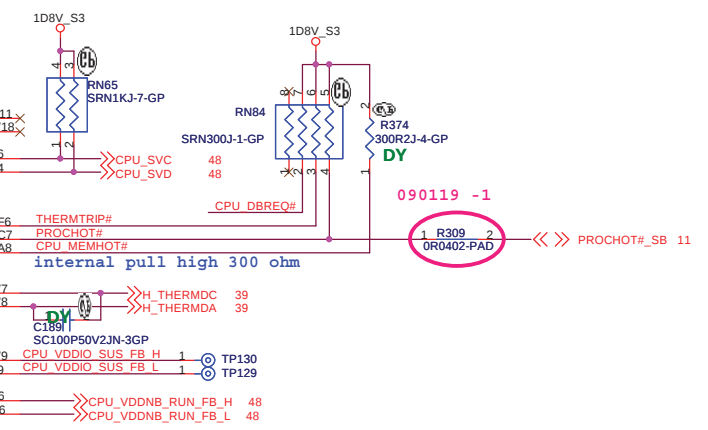
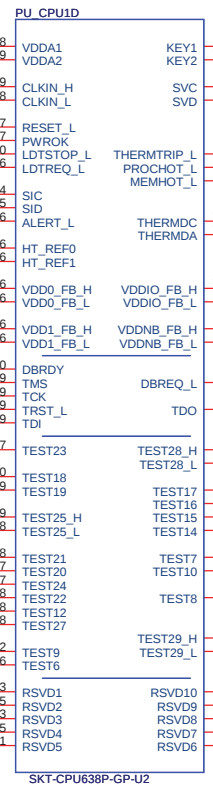
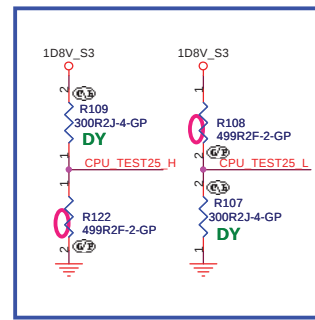


081223 SC

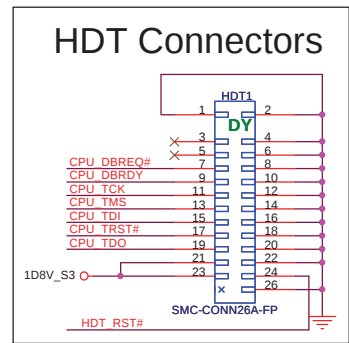


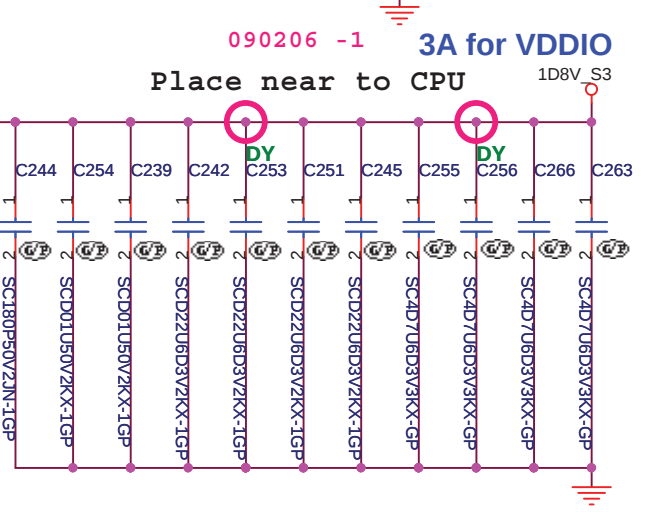
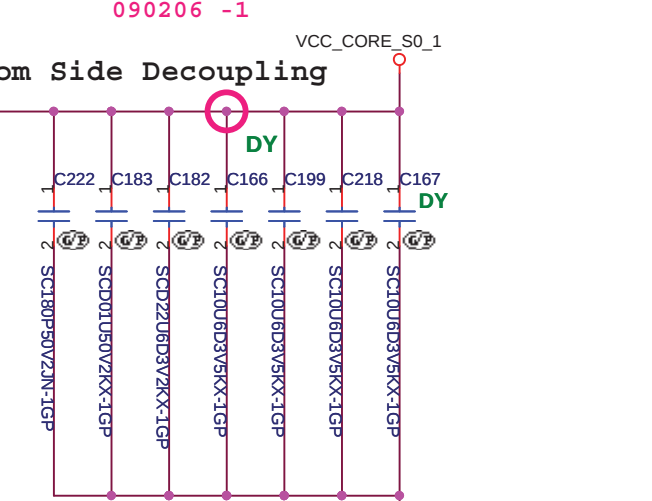
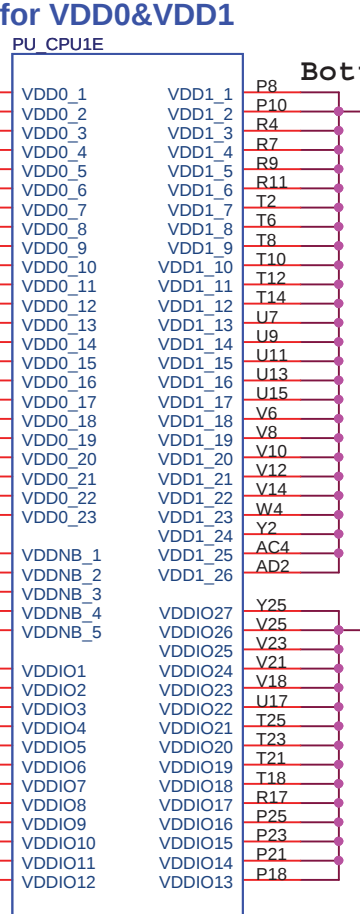
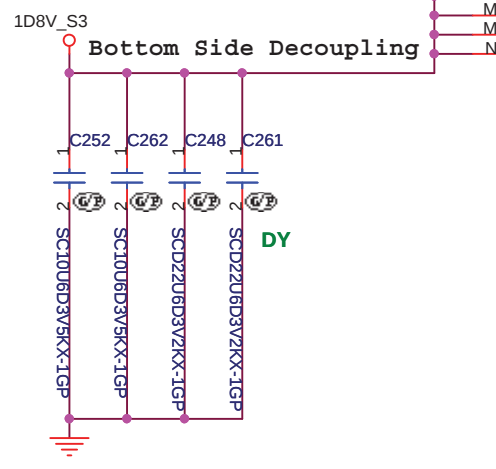
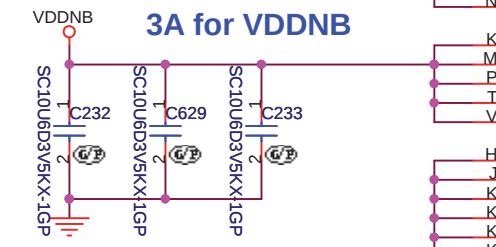
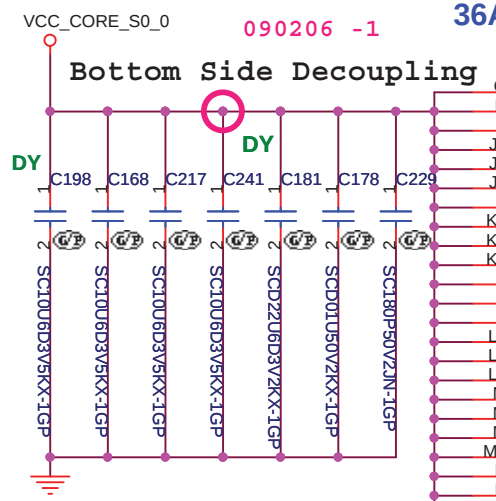
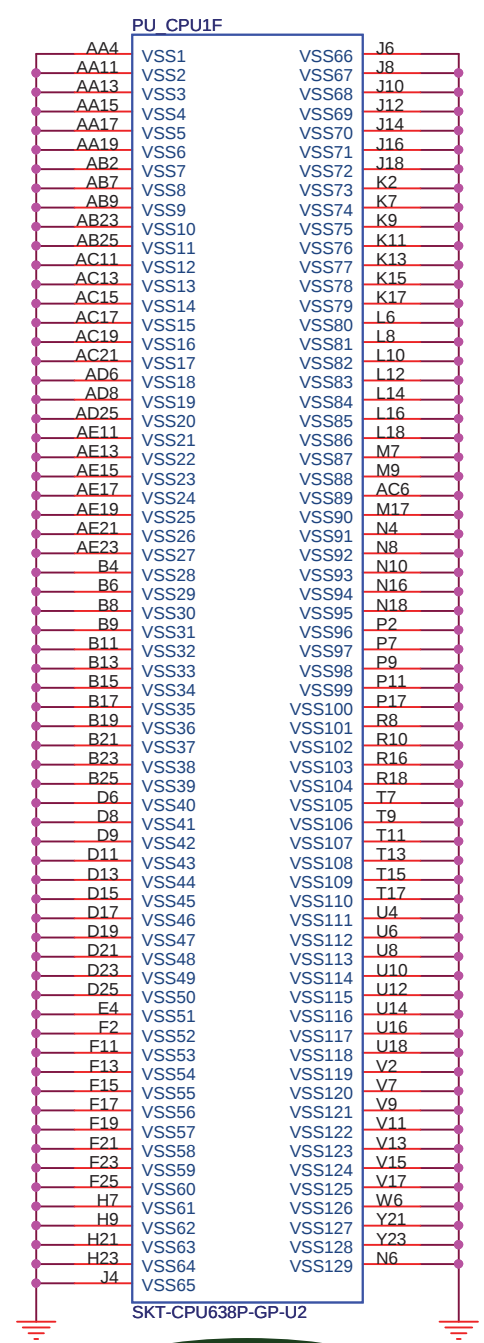
62 10055.111
2ND = 62.10055.251
090109 SC

090113 -1



LAYOUT: Route FBCLKOUT_H/L
differentially impedance 80

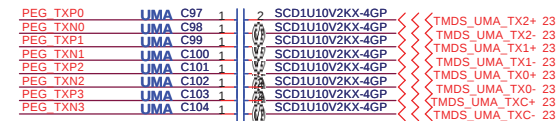
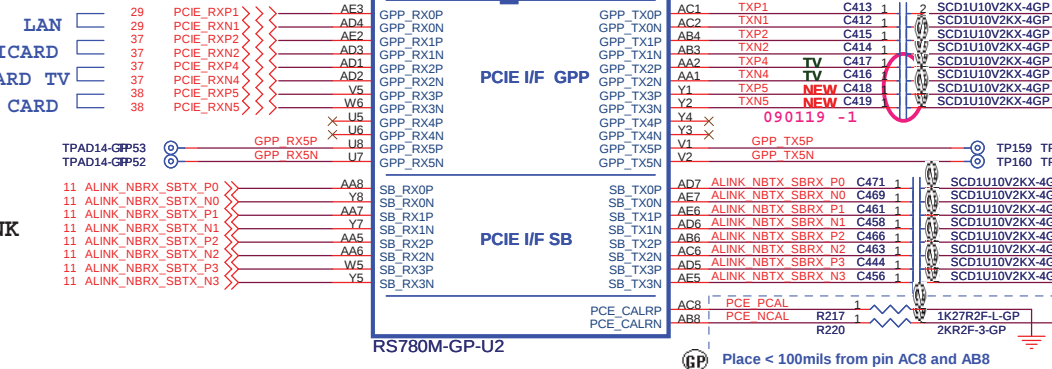
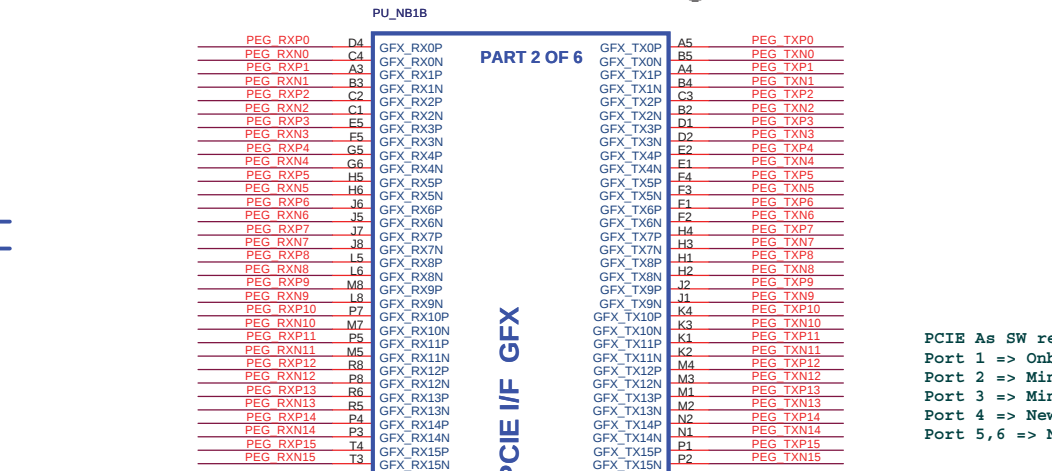




62.10055.111
2ND = 62.10055.251
090109 SC

<Core Design>

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
CPU_Power_(4/4)		
Size	Document Number	Rev
A4	JM70-PU	-2
Date	Monday, March 02, 2009	Sheet 7 of 56



RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2, TX3, AUX0, HPD0
DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1

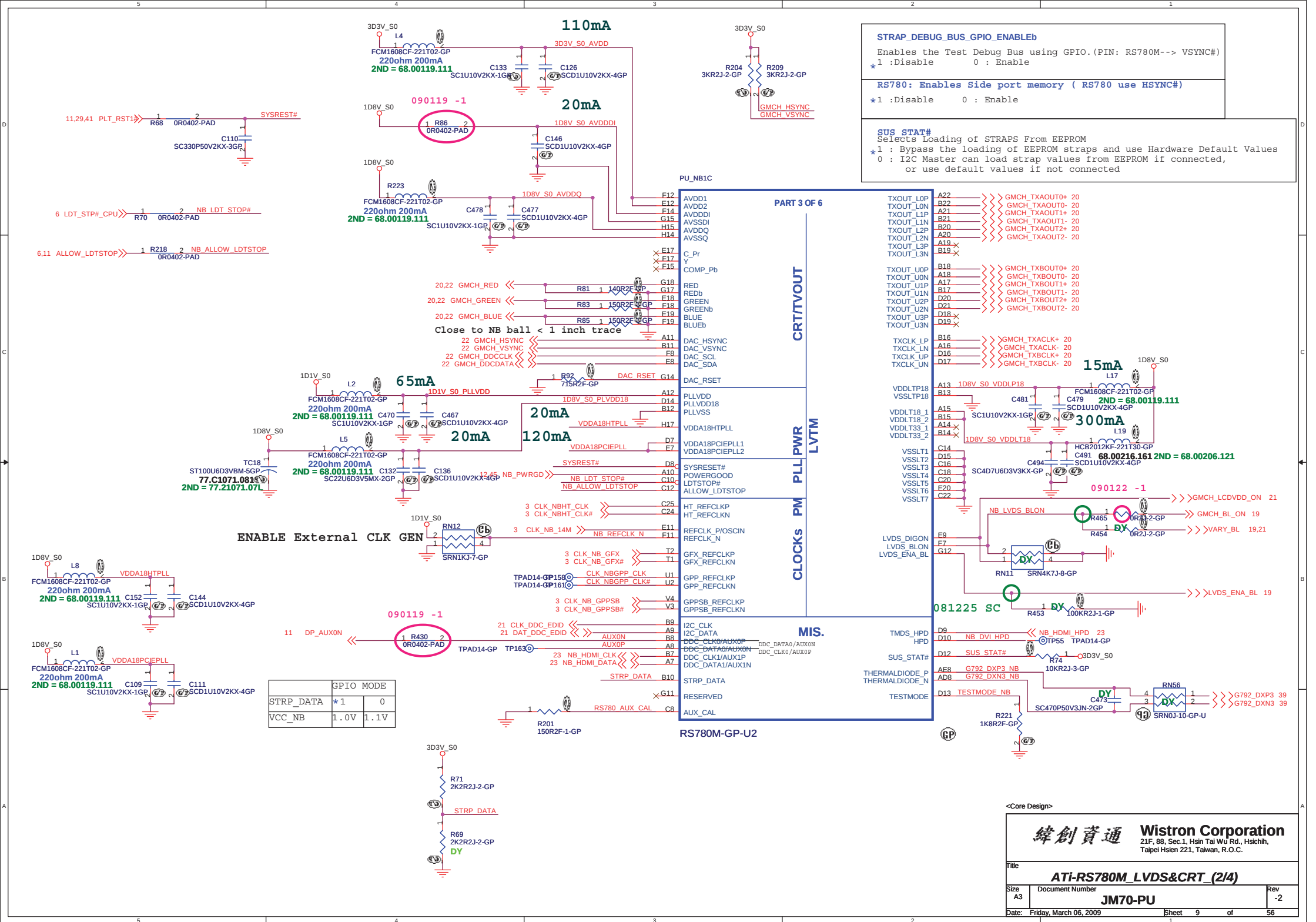
PCIE As SW request 11/17
Port 1 => Onboard LAN
Port 2 => Mini Card WLAN
Port 3 => Mini Card#2
Port 4 => New Card
Port 5, 6 => NC

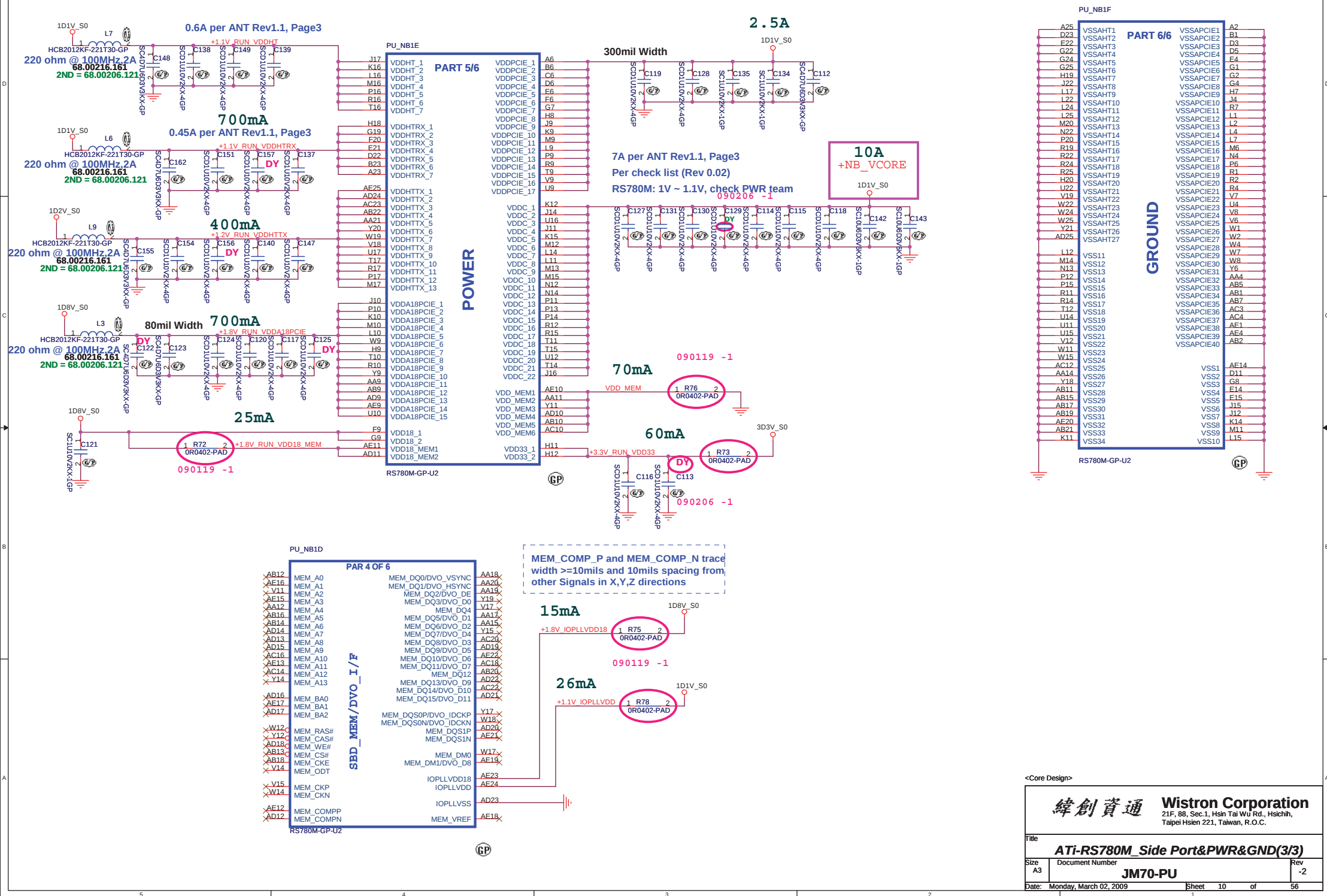


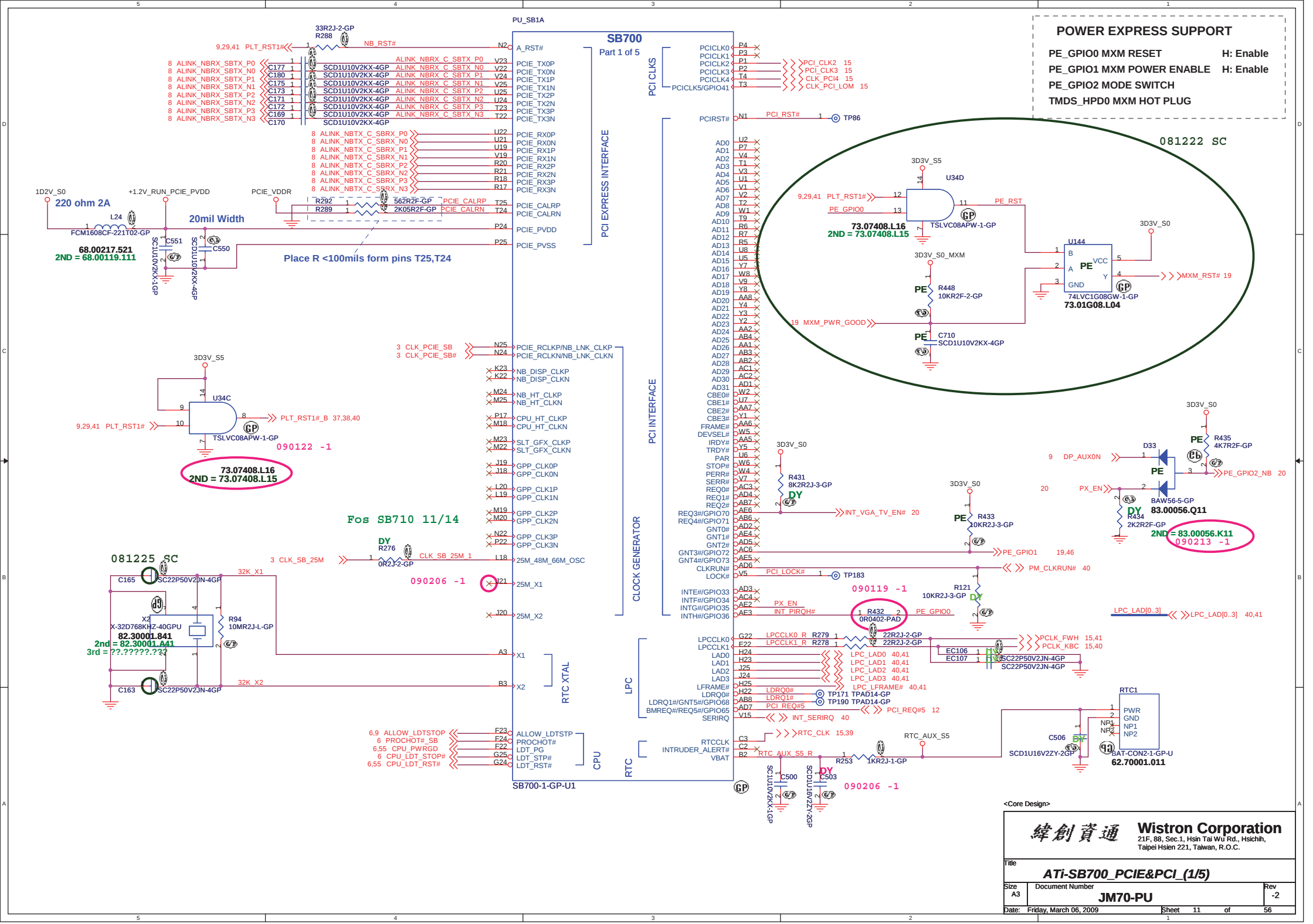
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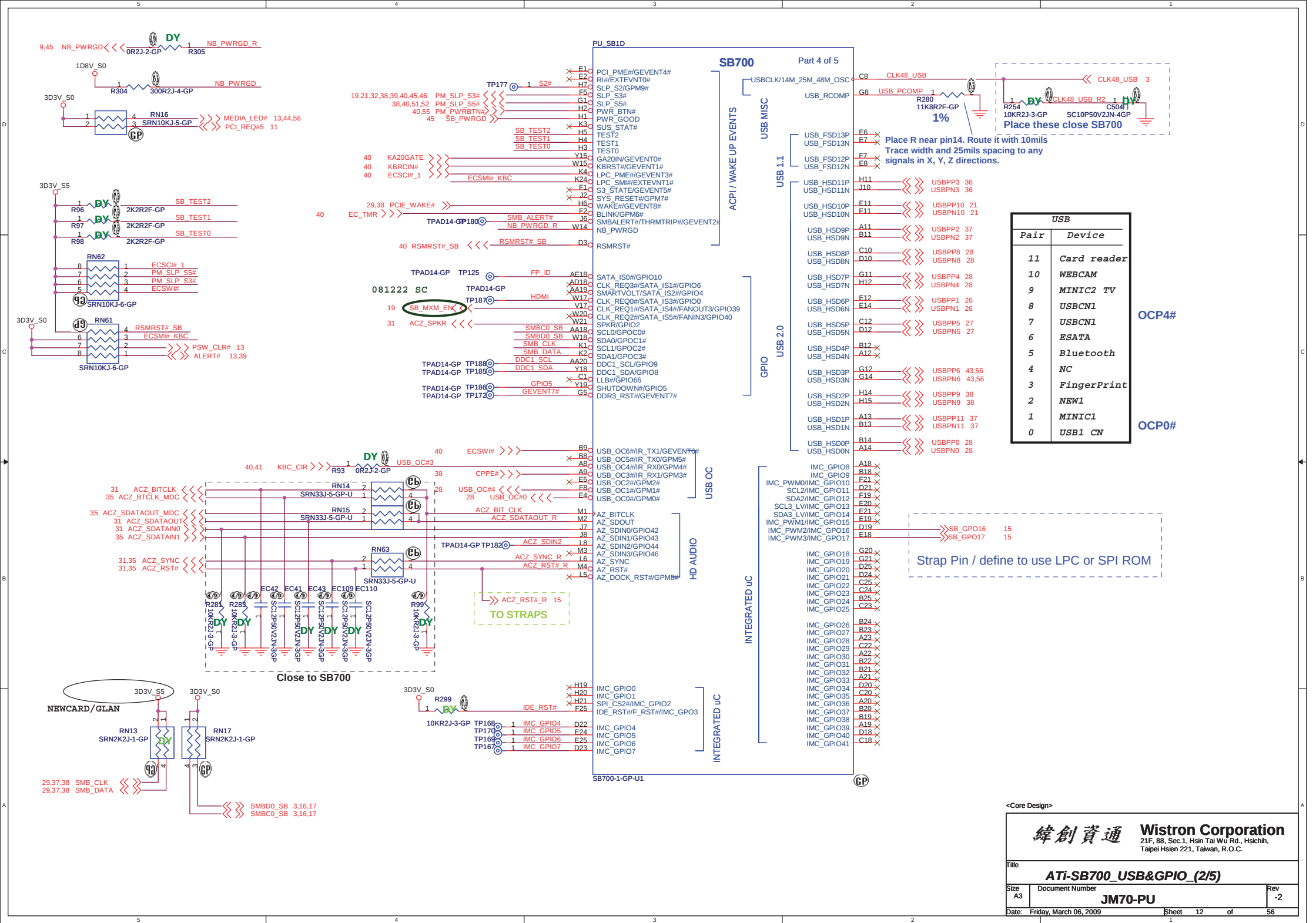
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Ati-RS780M_HT LINK&PCIE(1/3)		
Size	Document Number	Rev	-2
A3	JM70-PU		
Date:	Friday, March 06, 2009	Sheet	8 of 56

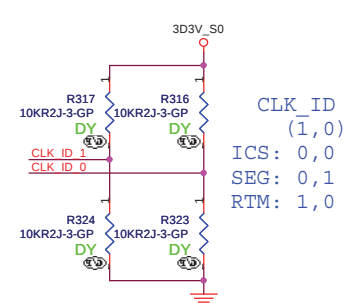
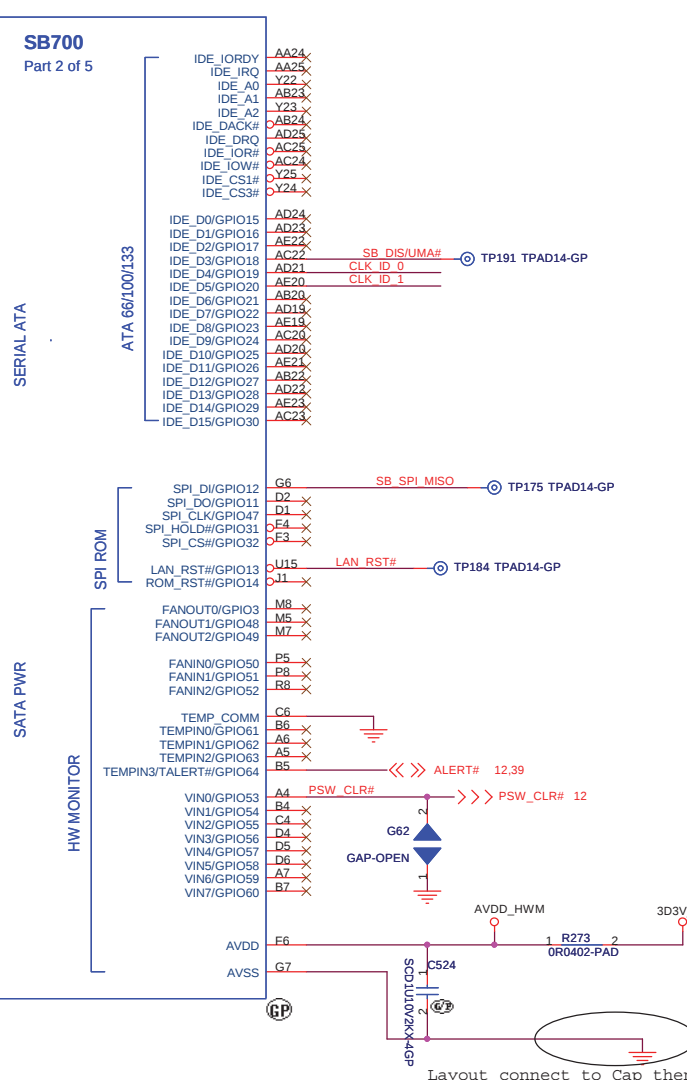
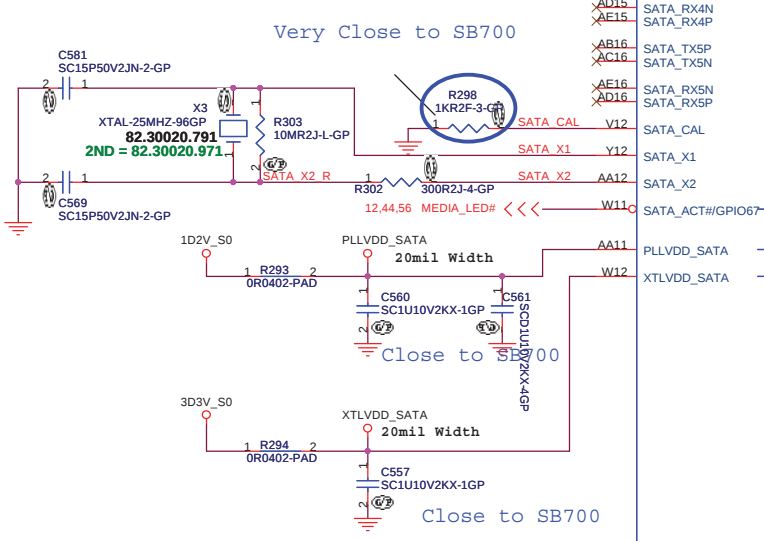
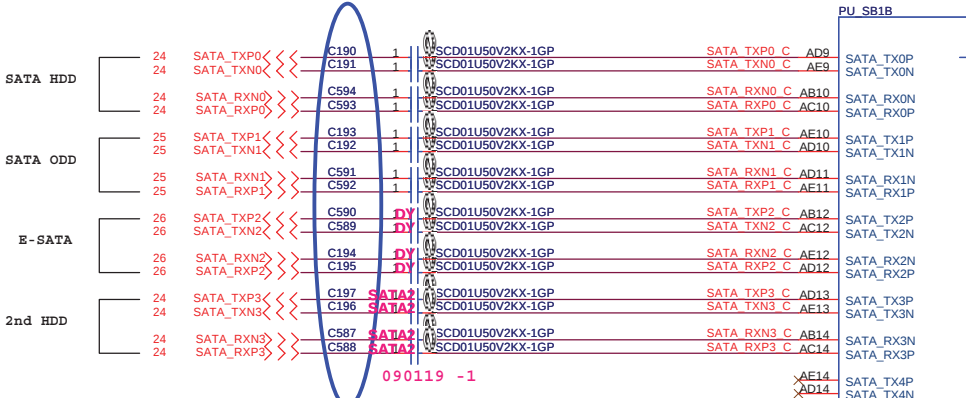


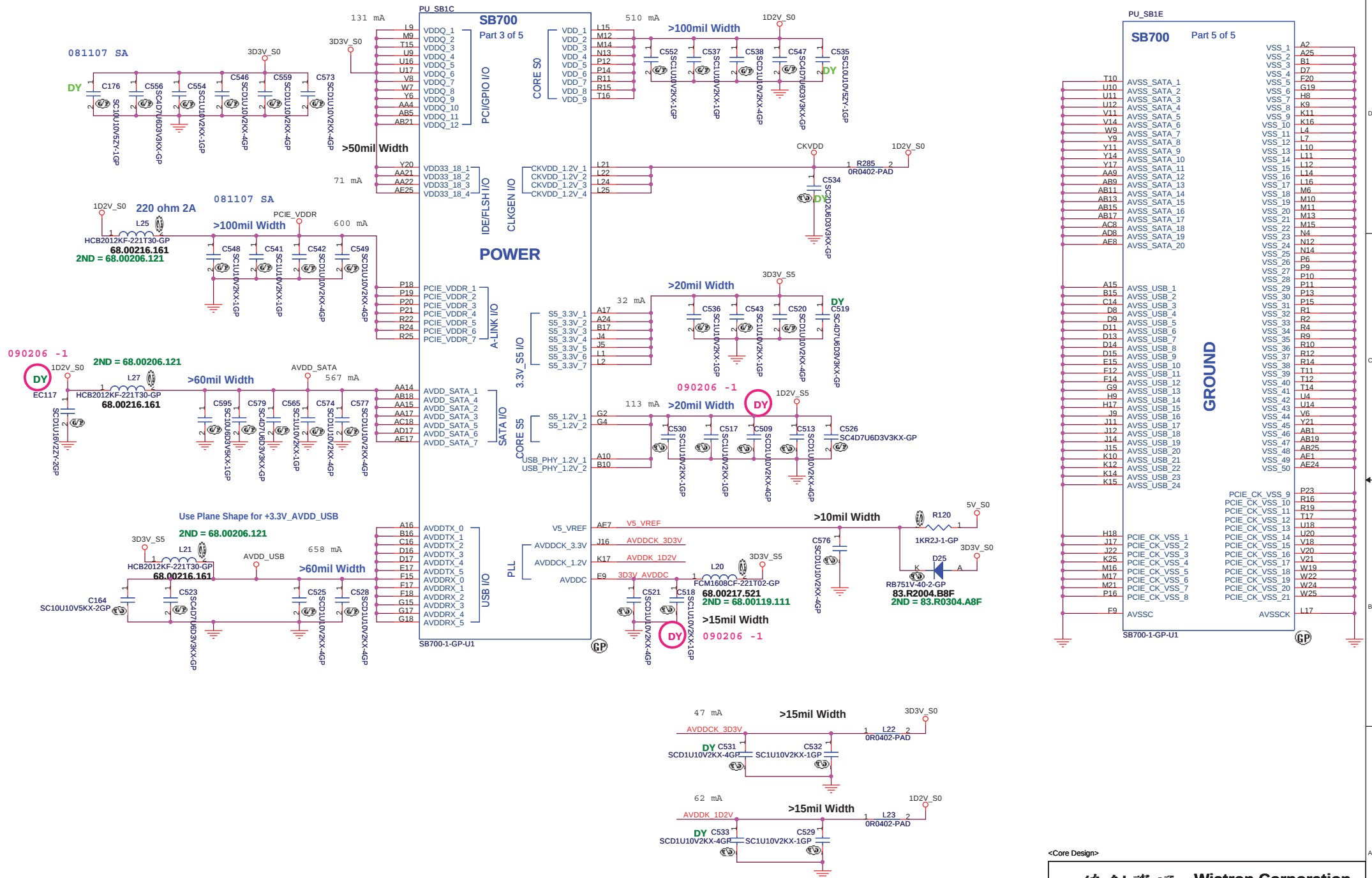




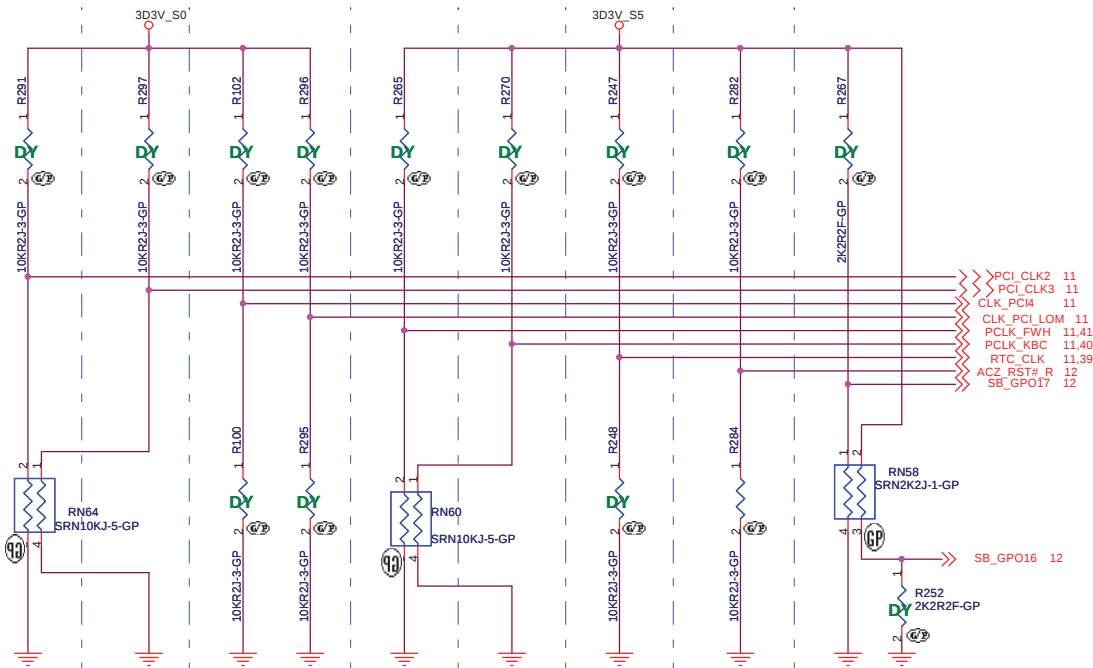


PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700





REQUIRED STRAPS
REQUIRED SYSTEM STRAPS



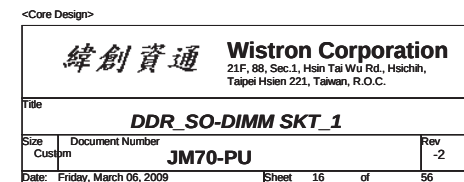
DEBUG STRAPS

	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]



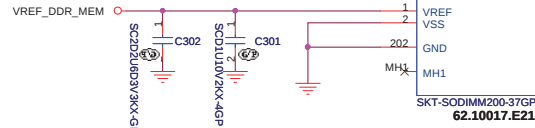
5,18 MEM_MB_ADD0 >> 102 A0
5,18 MEM_MB_ADD1 >> 101 A1
5,18 MEM_MB_ADD2 >> 100 A2
5,18 MEM_MB_ADD3 >> 98 A3
5,18 MEM_MB_ADD4 >> 97 A4
5,18 MEM_MB_ADD5 >> 94 A5
5,18 MEM_MB_ADD6 >> 92 A6
5,18 MEM_MB_ADD7 >> 93 A7
5,18 MEM_MB_ADD8 >> 91 A8
5,18 MEM_MB_ADD9 >> 105 A9
5,18 MEM_MB_ADD10 >> 90 A10/AP
5,18 MEM_MB_ADD11 >> 89 A11
5,18 MEM_MB_ADD12 >> 116 A12
5,18 MEM_MB_ADD13 >> 86 A13
5,18 MEM_MB_ADD14 >> 84 A14
5,18 MEM_MB_ADD15 >> 85 A15
5,18 MEM_MB_BANK2 >> A16/BA2
5,18 MEM_MB_BANK0 >> 107 BA0
5,18 MEM_MB_BANK1 >> 106 BA1

5 MEM_MB_DATA0 >> 5 DQ0
5 MEM_MB_DATA1 >> 7 DQ1
5 MEM_MB_DATA2 >> 17 DQ2
5 MEM_MB_DATA3 >> 19 DQ3
5 MEM_MB_DATA4 >> 4 DQ4
5 MEM_MB_DATA5 >> 6 DQ5
5 MEM_MB_DATA6 >> 14 DQ6
5 MEM_MB_DATA7 >> 16 DQ7
5 MEM_MB_DATA8 >> 23 DQ8
5 MEM_MB_DATA9 >> 25 DQ9
5 MEM_MB_DATA10 >> 35 DQ10
5 MEM_MB_DATA11 >> 37 DQ11
5 MEM_MB_DATA12 >> 20 DQ12
5 MEM_MB_DATA13 >> 22 DQ13
5 MEM_MB_DATA14 >> 36 DQ14
5 MEM_MB_DATA15 >> 38 DQ15
5 MEM_MB_DATA16 >> 43 DQ16
5 MEM_MB_DATA17 >> 45 DQ17
5 MEM_MB_DATA18 >> 55 DQ18
5 MEM_MB_DATA19 >> 57 DQ19
5 MEM_MB_DATA20 >> 44 DQ20
5 MEM_MB_DATA21 >> 46 DQ21
5 MEM_MB_DATA22 >> 58 DQ22
5 MEM_MB_DATA23 >> 61 DQ23
5 MEM_MB_DATA24 >> 58 DQ24
5 MEM_MB_DATA25 >> 63 DQ25
5 MEM_MB_DATA26 >> 73 DQ26
5 MEM_MB_DATA27 >> 75 DQ27
5 MEM_MB_DATA28 >> 62 DQ28
5 MEM_MB_DATA29 >> 64 DQ29
5 MEM_MB_DATA30 >> 74 DQ30
5 MEM_MB_DATA31 >> 76 DQ31
5 MEM_MB_DATA32 >> 123 DQ32
5 MEM_MB_DATA33 >> 125 DQ33
5 MEM_MB_DATA34 >> 135 DQ34
5 MEM_MB_DATA35 >> 137 DQ35
5 MEM_MB_DATA36 >> 124 DQ36
5 MEM_MB_DATA37 >> 126 DQ37
5 MEM_MB_DATA38 >> 134 DQ38
5 MEM_MB_DATA39 >> 136 DQ39
5 MEM_MB_DATA40 >> 141 DQ40
5 MEM_MB_DATA41 >> 143 DQ41
5 MEM_MB_DATA42 >> 151 DQ42
5 MEM_MB_DATA43 >> 153 DQ43
5 MEM_MB_DATA44 >> 140 DQ44
5 MEM_MB_DATA45 >> 142 DQ45
5 MEM_MB_DATA46 >> 152 DQ46
5 MEM_MB_DATA47 >> 154 DQ47
5 MEM_MB_DATA48 >> 157 DQ48
5 MEM_MB_DATA49 >> 159 DQ49
5 MEM_MB_DATA50 >> 173 DQ50
5 MEM_MB_DATA51 >> 175 DQ51
5 MEM_MB_DATA52 >> 158 DQ52
5 MEM_MB_DATA53 >> 160 DQ53
5 MEM_MB_DATA54 >> 174 DQ54
5 MEM_MB_DATA55 >> 176 DQ55
5 MEM_MB_DATA56 >> 179 DQ56
5 MEM_MB_DATA57 >> 181 DQ57
5 MEM_MB_DATA58 >> 189 DQ58
5 MEM_MB_DATA59 >> 191 DQ59
5 MEM_MB_DATA60 >> 180 DQ60
5 MEM_MB_DATA61 >> 182 DQ61
5 MEM_MB_DATA62 >> 192 DQ62
5 MEM_MB_DATA63 >> 194 DQ63

5 MEM_MB_DQS0_N >> 11 DQS0#
5 MEM_MB_DQS1_N >> 29 DQS1#
5 MEM_MB_DQS2_N >> 49 DQS2#
5 MEM_MB_DQS3_N >> 68 DQS3#
5 MEM_MB_DQS4_N >> 129 DQS4#
5 MEM_MB_DQS5_N >> 146 DQS5#
5 MEM_MB_DQS6_N >> 167 DQS6#
5 MEM_MB_DQS7_N >> 186 DQS7#

5 MEM_MB_DQS0_P >> 13 DQS0
5 MEM_MB_DQS1_P >> 31 DQS1
5 MEM_MB_DQS2_P >> 51 DQS2
5 MEM_MB_DQS3_P >> 70 DQS3
5 MEM_MB_DQS4_P >> 131 DQS4
5 MEM_MB_DQS5_P >> 148 DQS5
5 MEM_MB_DQS6_P >> 169 DQS6
5 MEM_MB_DQS7_P >> 188 DQS7

5,18 MEM_MB0_ODT0 >> 114 OTD0
5,18 MEM_MB0_ODT1 >> 119 OTD1



Place C2.2uF and 0.1uF < 500mils from DDR connector

HI 9.2mm

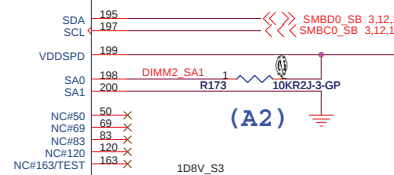
62.10017.E21

081225 SC

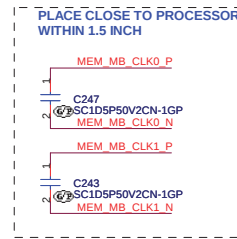
ZND = 62.10017.071

NORMAL TYPE

PU DM2
RAS# 108 A0
WE# 109 A1
CAS# 113 A2
CS0# 110 A3
CS1# 115 A4
CKE0 79 A5
CKE1 80 A6
CK0 30 A7
CK0# 32 A8
CK1 164 A9
CK1# 166 A10/AP
DM0 10 A11
DM1 26 A12
DM2 52 A13
DM3 130 A14
DM4 147 A15
DM5 170 A16/BA2
DM6 185 BA0
DM7 185 BA1



SDA 195
SCL 197
VDDSPD 199
SA0 198
SA1 200
NC#50 50
NC#69 69
NC#83 83
NC#120 120
NC#163/TEST 163
VDD 81
VDD 82
VDD 87
VDD 88
VDD 95
VDD 96
VDD 103
VDD 104
VDD 111
VDD 112
VDD 117
VDD 118
VSS 3
VSS 8
VSS 9
VSS 12
VSS 15
VSS 18
VSS 21
VSS 24
VSS 27
VSS 28
VSS 33
VSS 34
VSS 38
VSS 40
VSS 41
VSS 42
VSS 47
VSS 48
VSS 53
VSS 54
VSS 59
VSS 60
VSS 65
VSS 66
VSS 71
VSS 72
VSS 77
VSS 78
VSS 121
VSS 122
VSS 127
VSS 128
VSS 132
VSS 133
VSS 138
VSS 139
VSS 144
VSS 145
VSS 149
VSS 150
VSS 155
VSS 156
VSS 161
VSS 162
VSS 165
VSS 168
VSS 171
VSS 172
VSS 173
VSS 174
VSS 177
VSS 178
VSS 183
VSS 184
VSS 187
VSS 190
VSS 193
VSS 196
GND 201
MH2 GP



<Core Design>

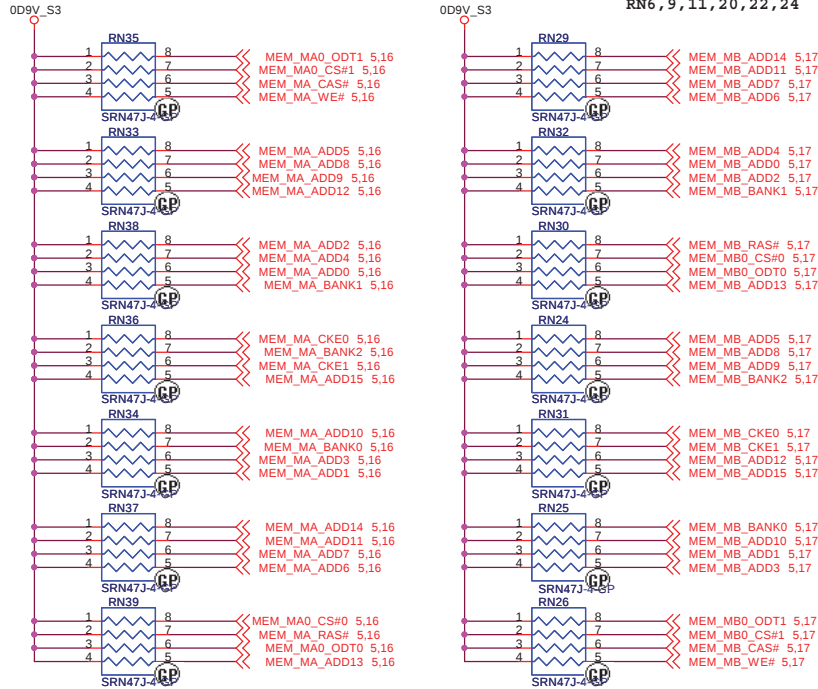
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			DDR_SO-DIMM SKT_2
Size	Document Number	Rev	
Custom	JM70-PU	-2	
Date:	Friday, March 06, 2009	Sheet	17 of 56

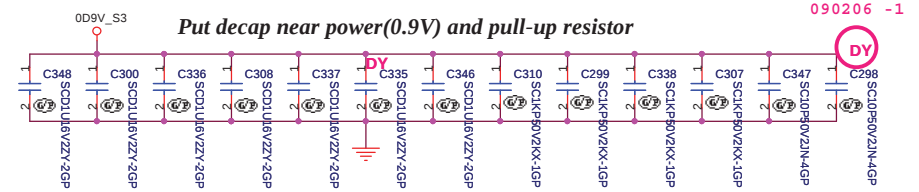
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

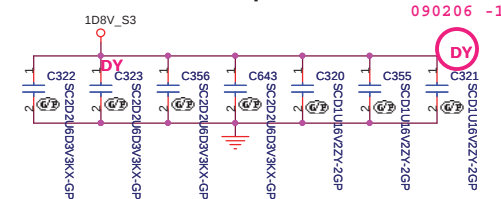
Net swap 11/14
RN6,9,11,20,22,24



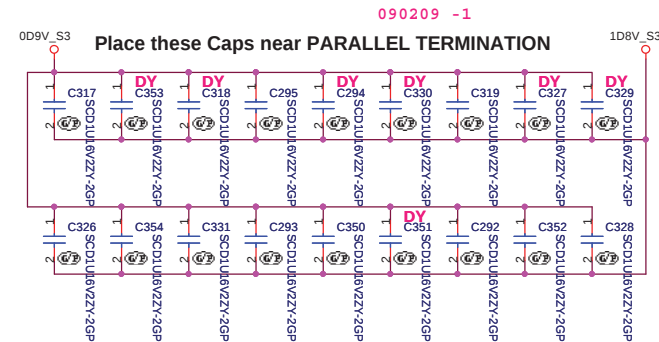
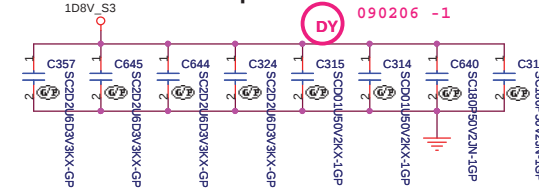
Decoupling Capacitor



Place these Caps near DM1



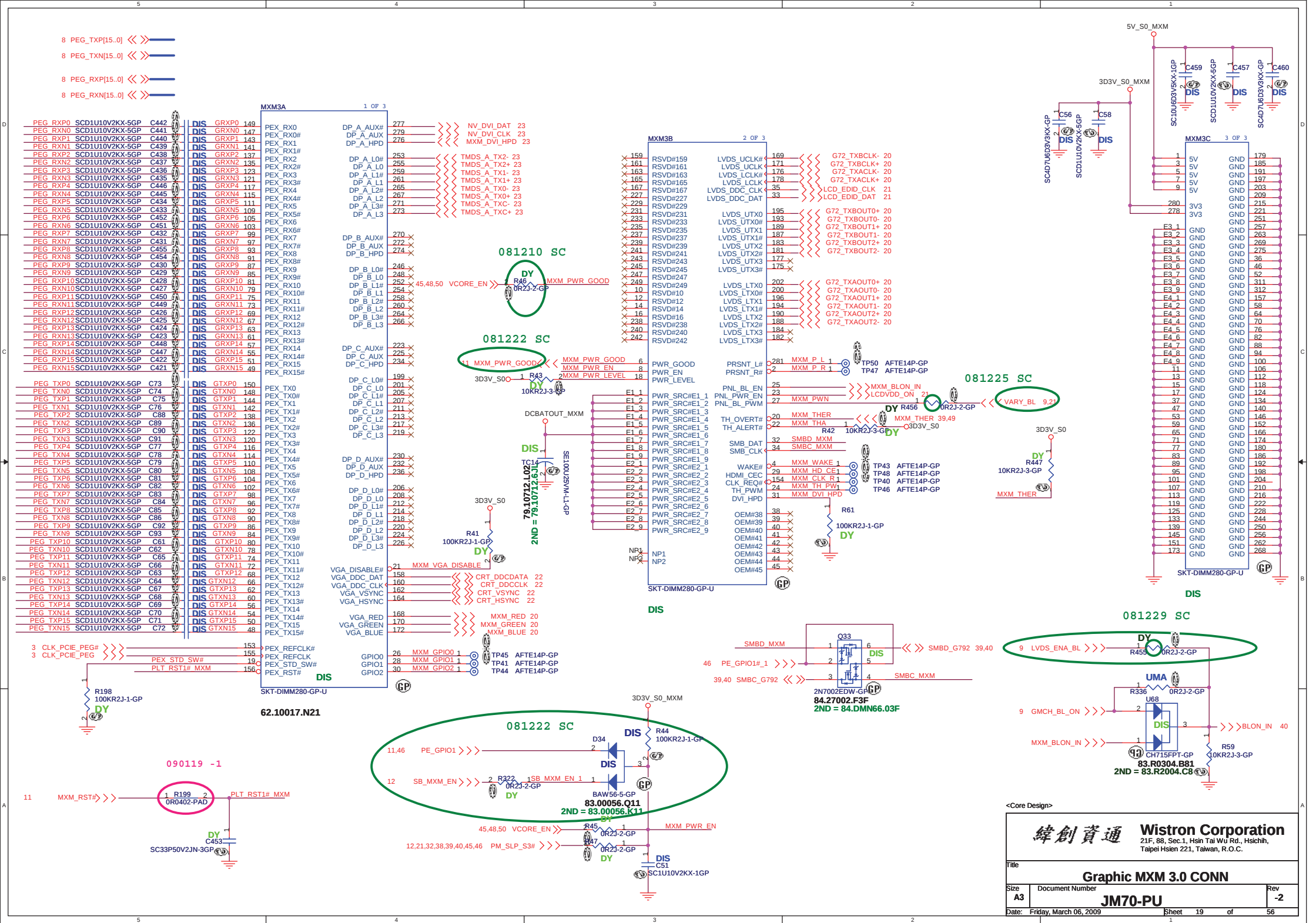
Place these Caps near DM2

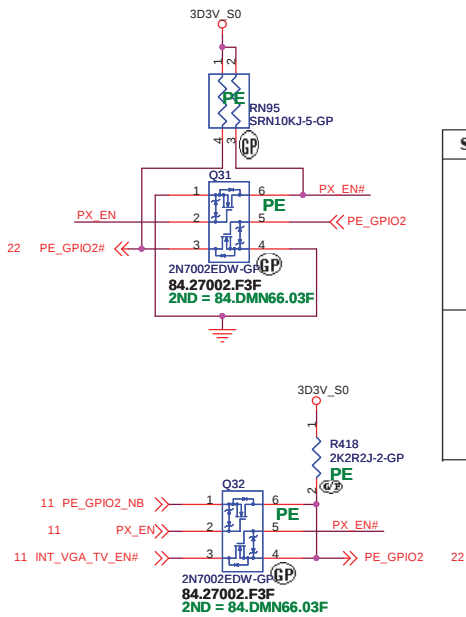


<Core Design>

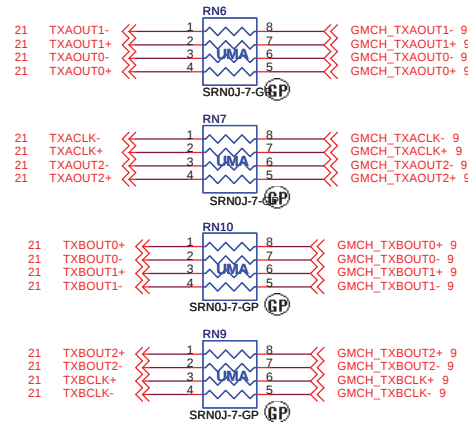
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title DDR DAMPING & TERMINATION		
Size A3	Document Number JM70-PU	Rev -2
Date: Friday, March 06, 2009	Sheet 18	of 56

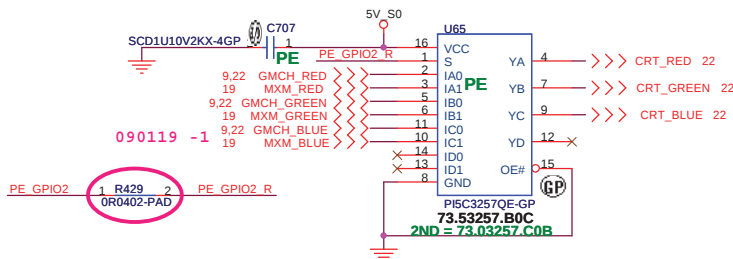




FUNCTION TABLE		
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

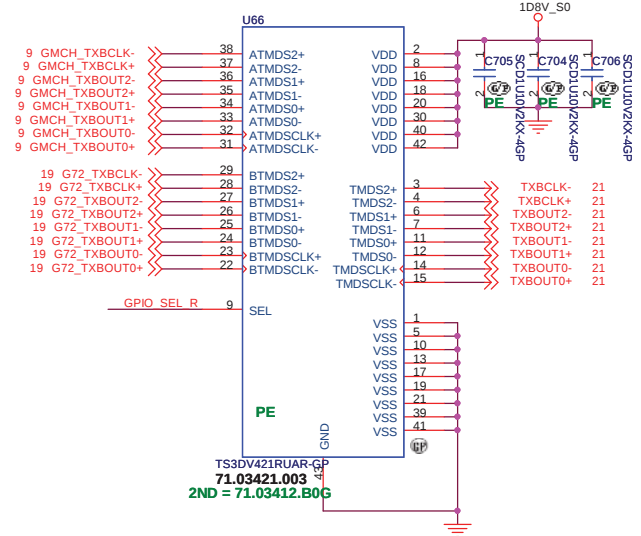
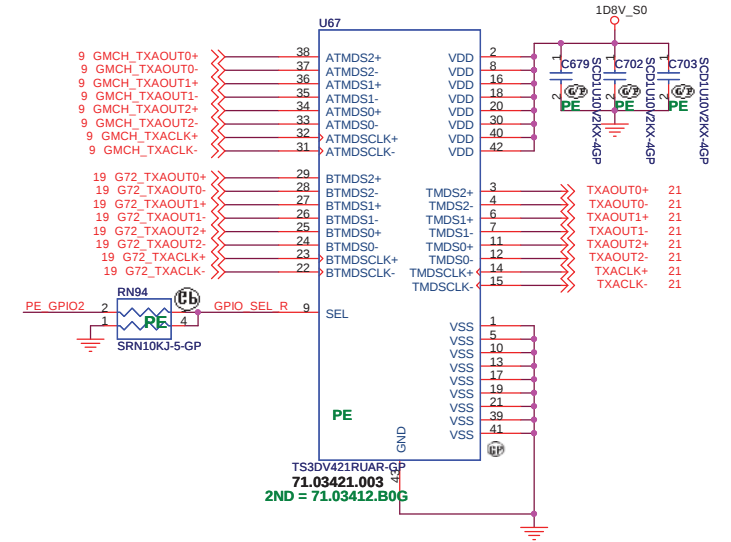


$\bar{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



DISPLAY SUPPORT TABLE

	PX_EN	PE_GPIO2_NB	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	0	X	0	IGP(LVDS,VGA,HDMI,DP)
MXM only mode	0	X	1	MXM(LVDS,VGA,HDMI,DP)
Power Express mode	1	0/1	X	*MXM(VGA,HDMI,DP); MXM/IGP(LVDS)
IGP + MXM	0	X	0	IGP(LVDS,VGA,HDMI)



<Core Design>

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Title

SWITCH

Size Document Number

JM70-PU

Date: Friday, March 06, 2009 Sheet 20 of 56

Rev

-2

LCD/INVERTER/CCD CONN

090302 -2

081222 SC

090211 -1 EMI

081225 SC

090119 -1

20.F1296.040
2ND = 20.F1096.040

081120 SC

Layout 40 mil

ACES-CONN40C-4-GP

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Size A3

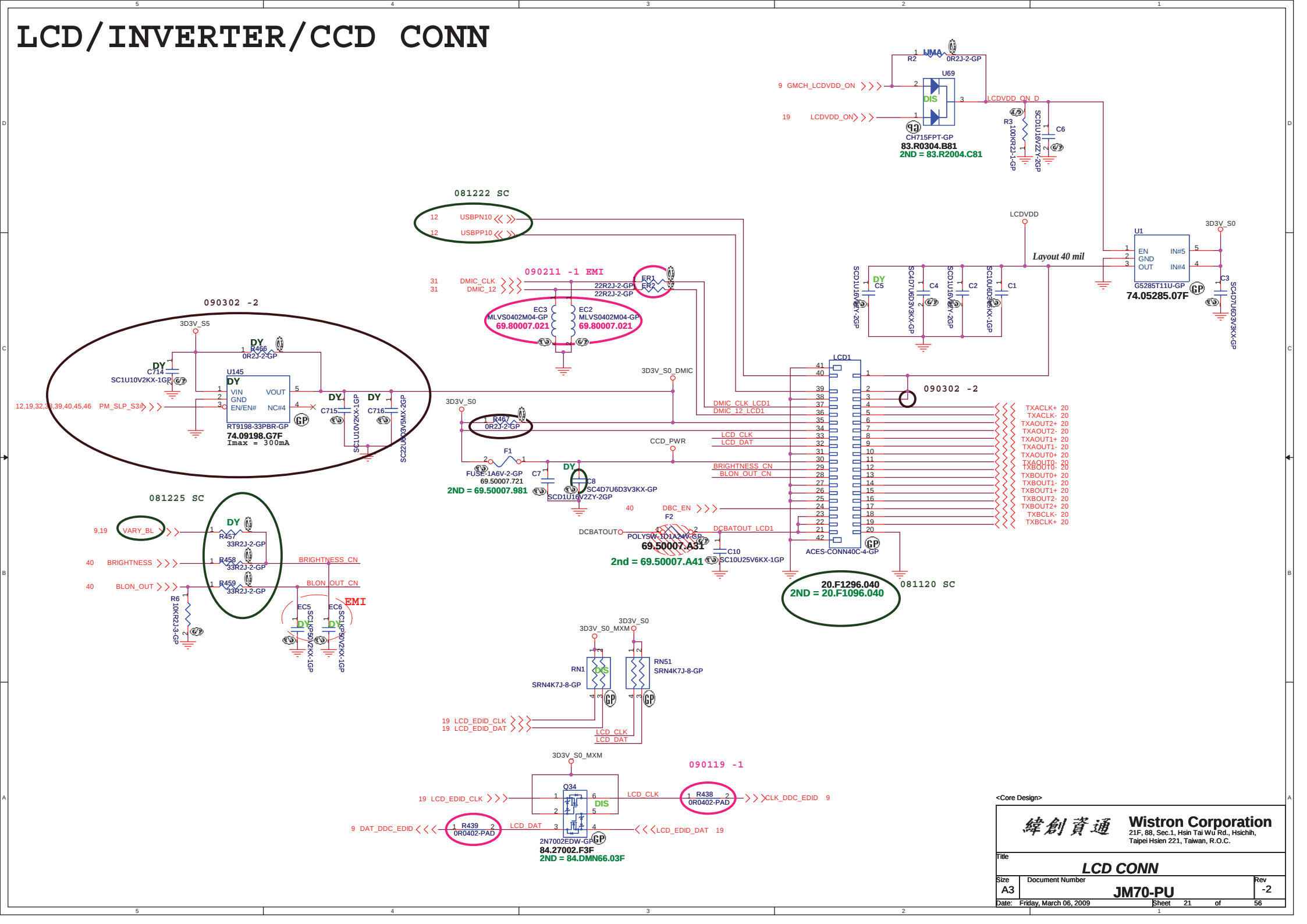
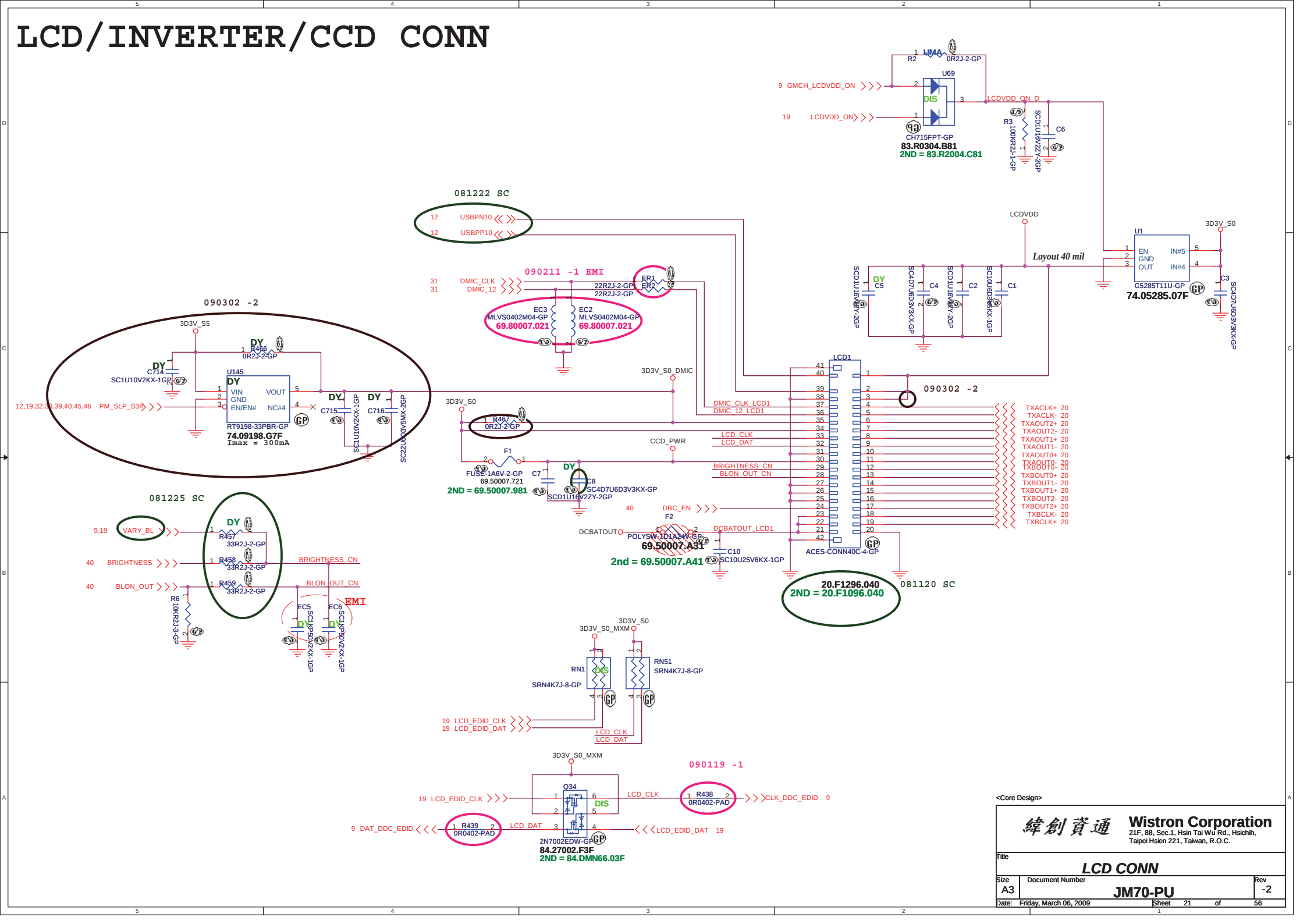
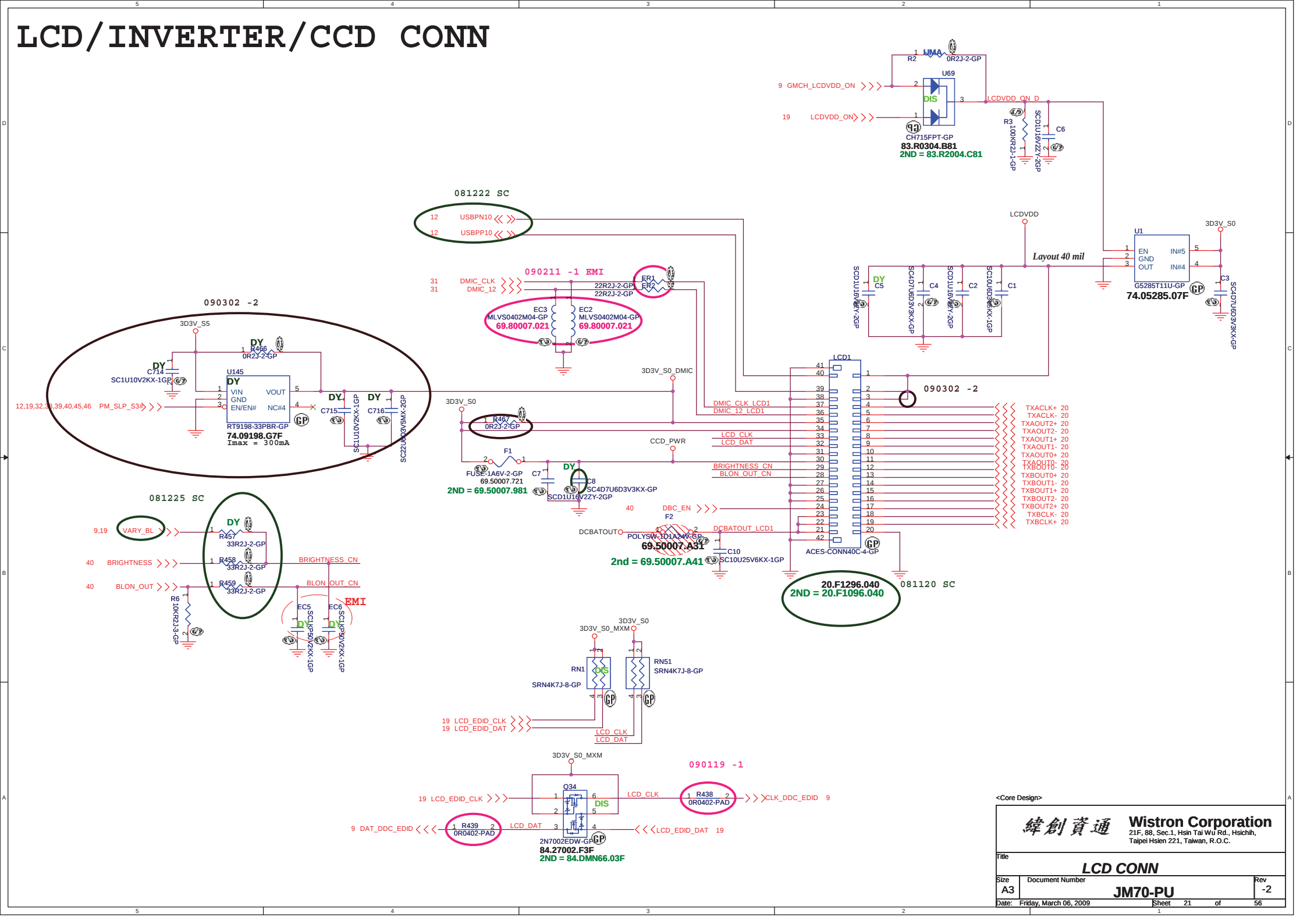
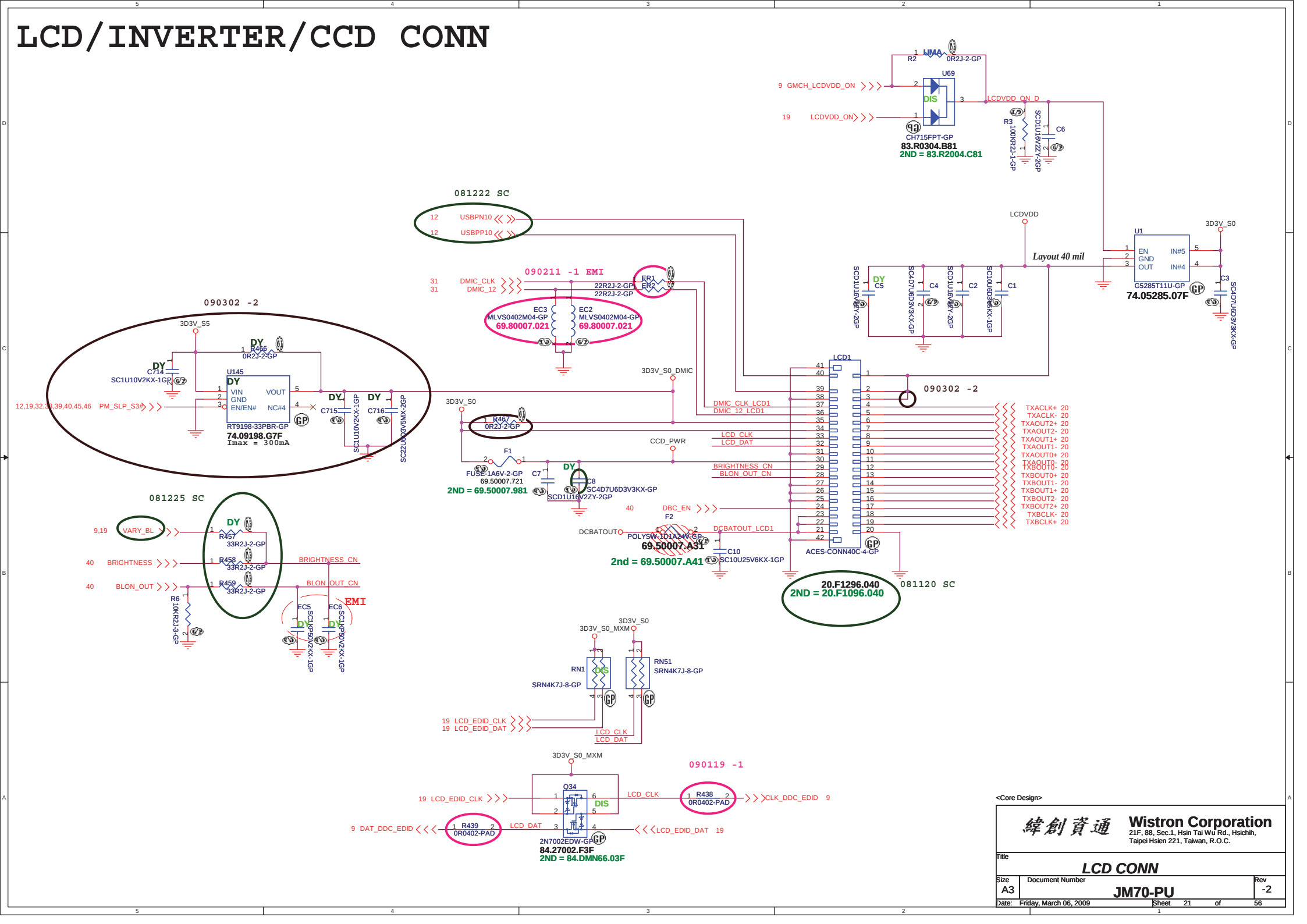
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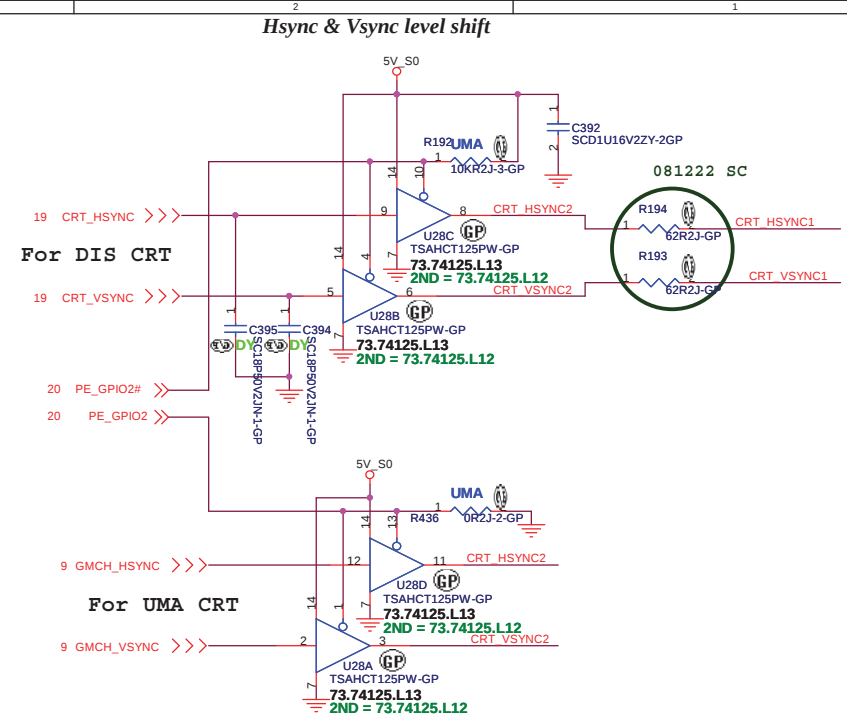
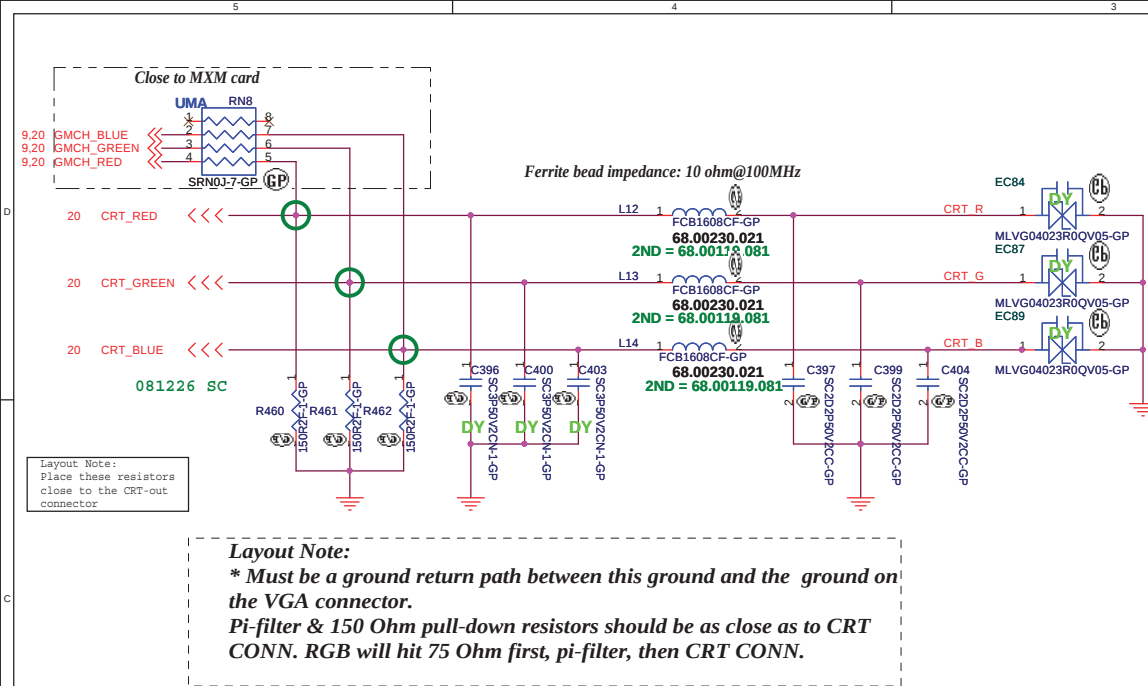
Date: Friday, March 06, 2009

Sheet 21 of 56

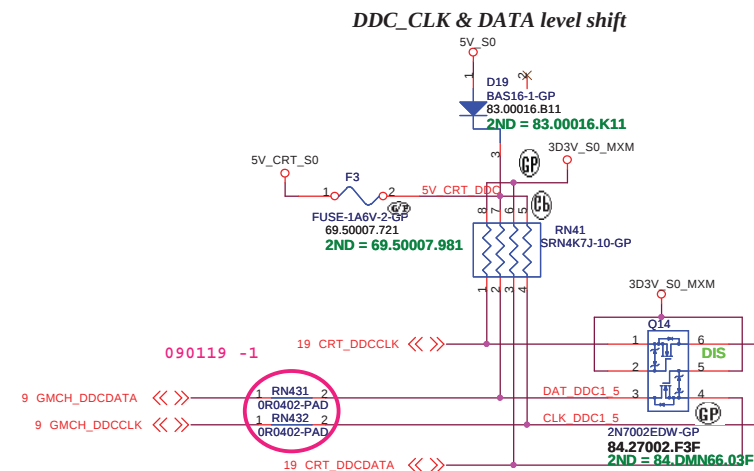
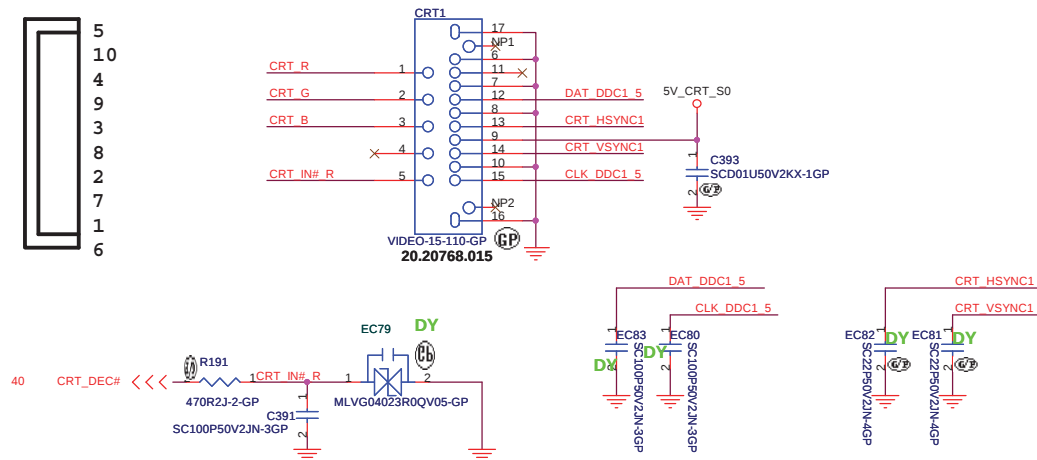
Rev -2

JM70-PU





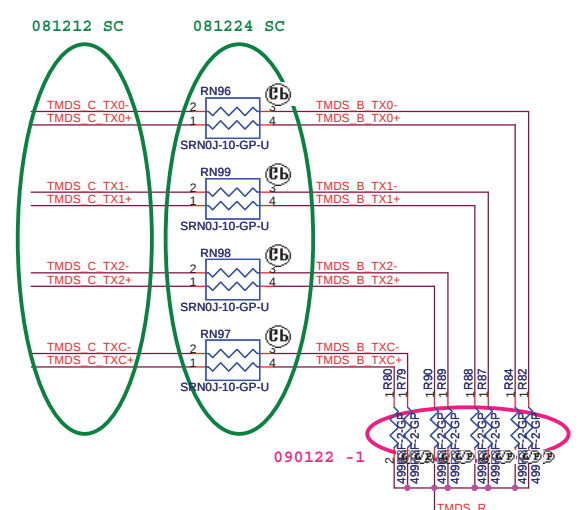
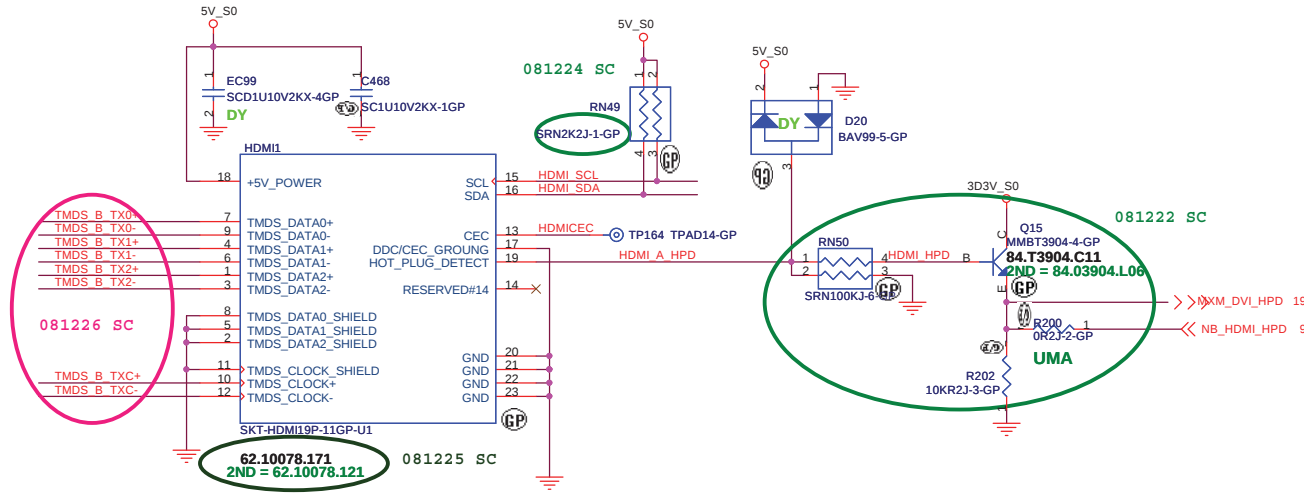
CRT I/F & CONNECTOR



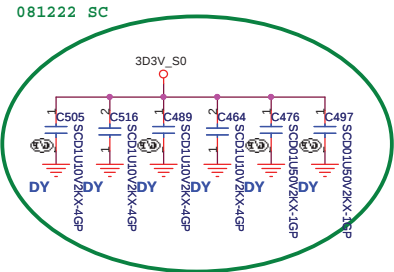
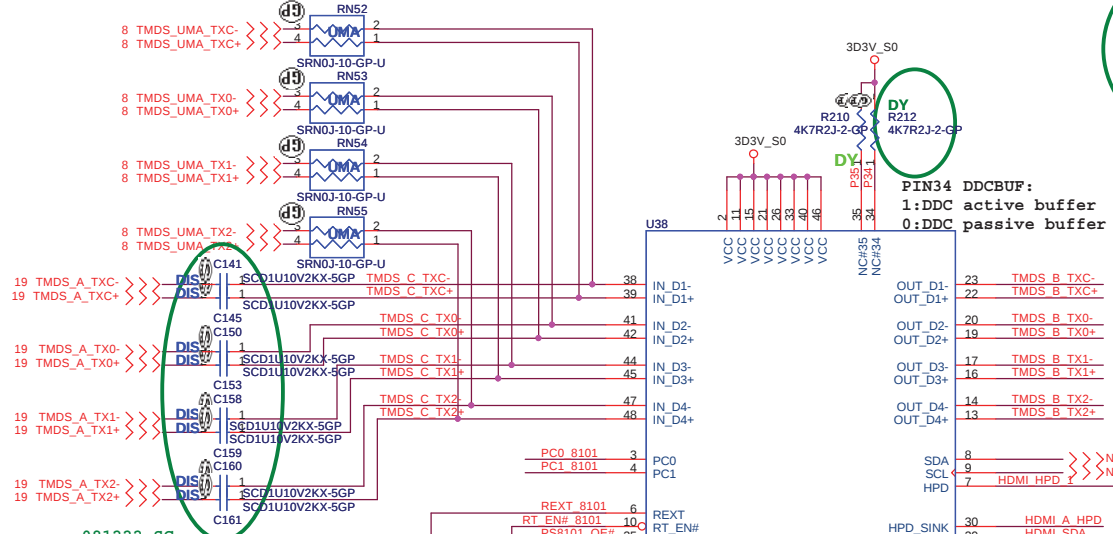
<Core Design>

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Title CRT Connector
Size Document Number JM70-PU
Date: Friday, March 06, 2009 Sheet 22 of 56

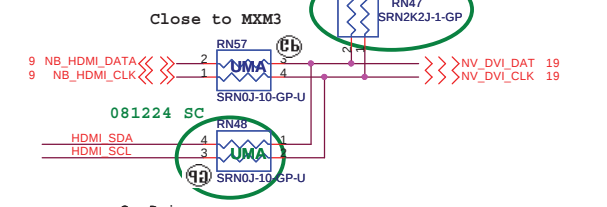
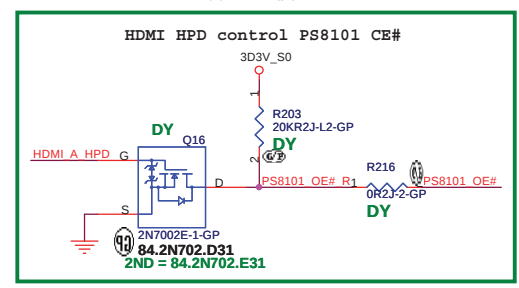
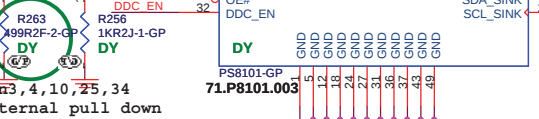
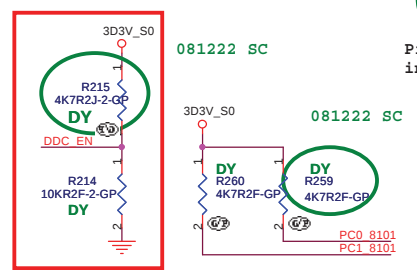
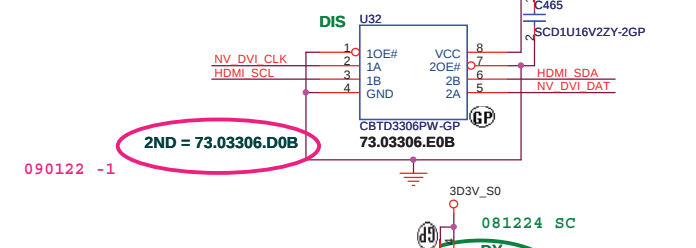


Place Near MXM3 Connector

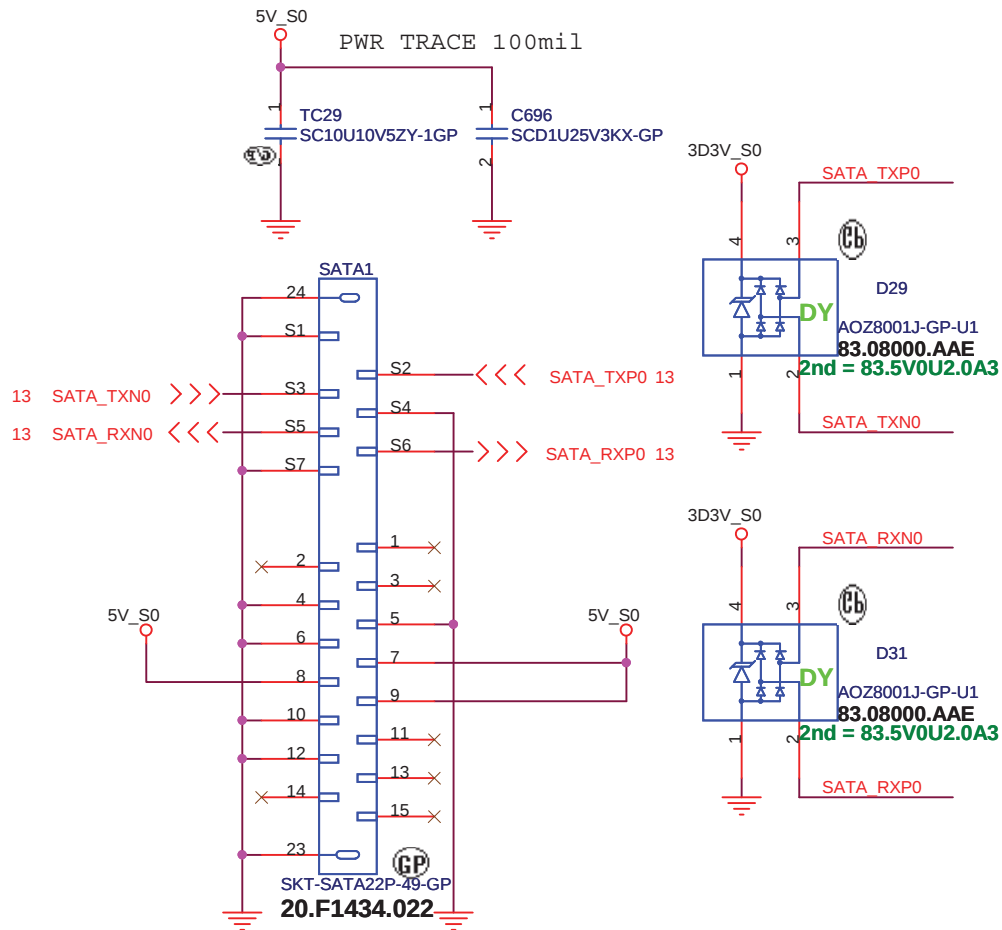


HDMI SM BUS LEVEL shifter

Close HDMI1

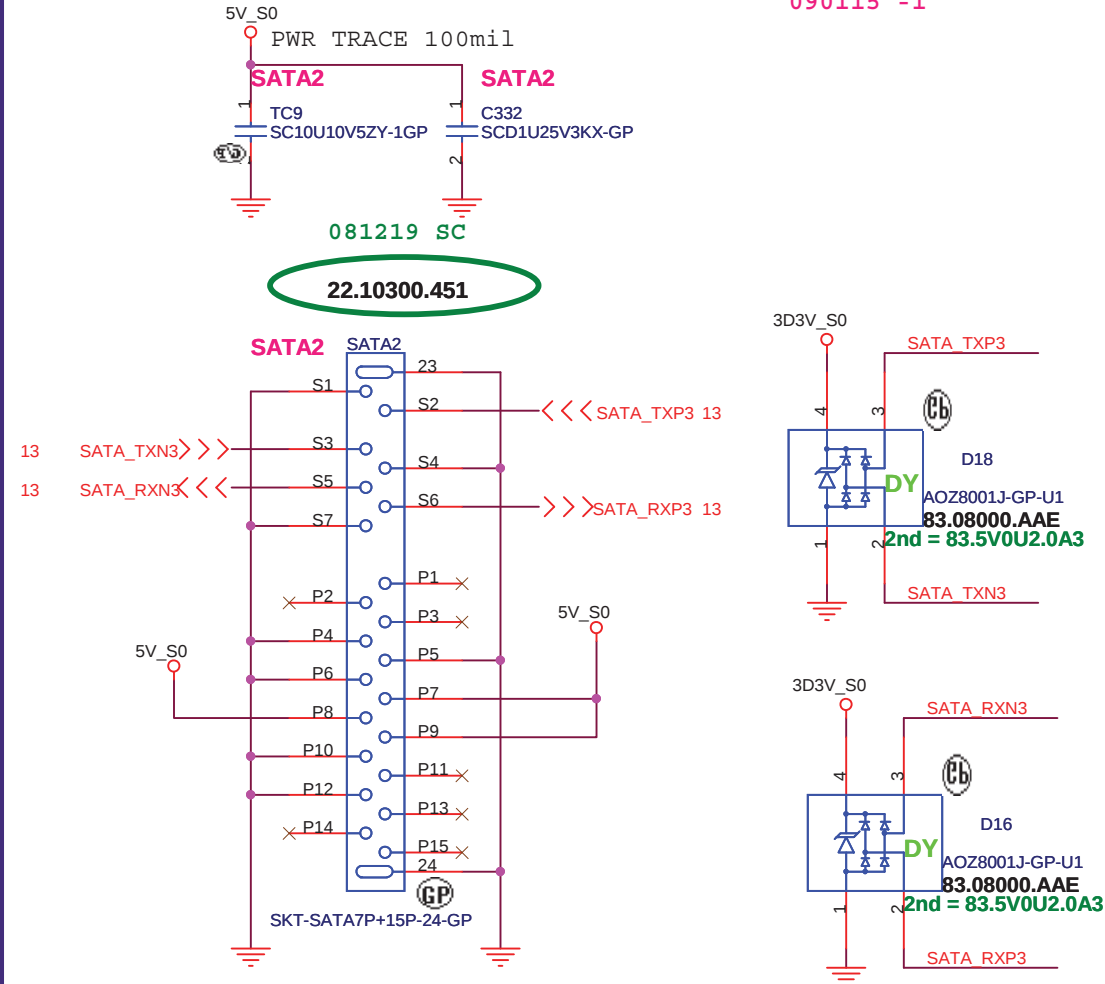


SATA HDD Connector



2ND SATA HDD Connector

090115 -1



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

HDD

Size

A4

Document Number

JM70-PU

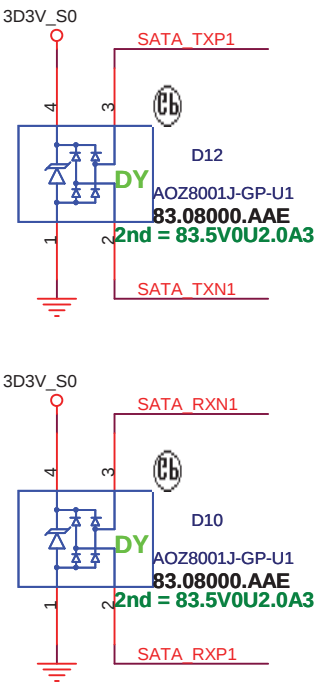
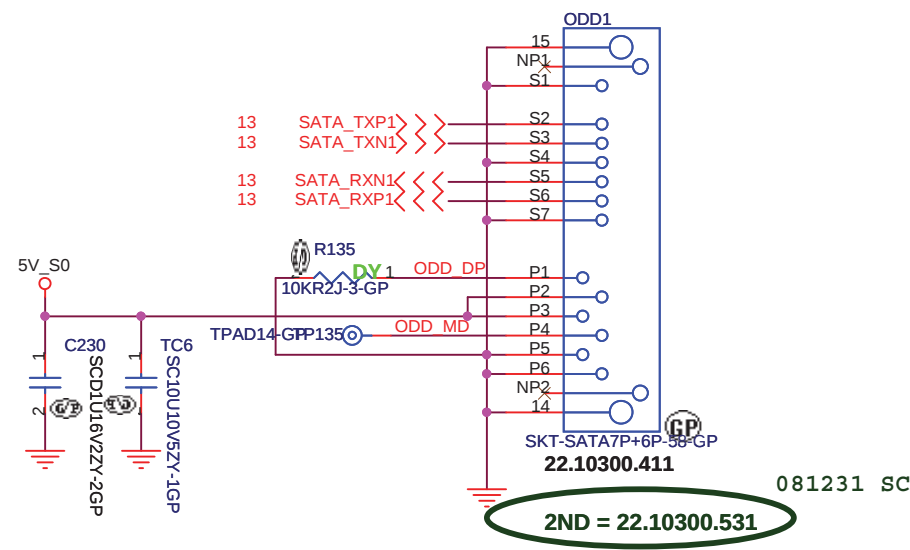
Rev

-2

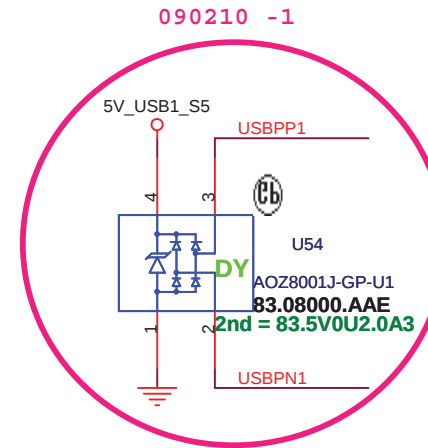
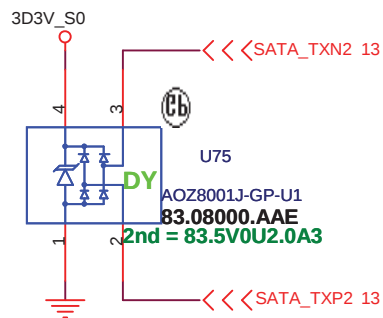
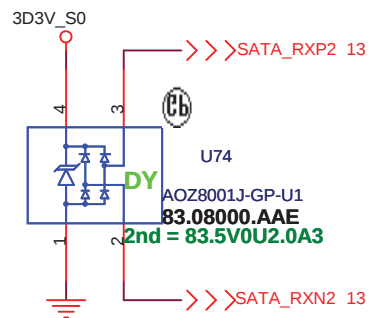
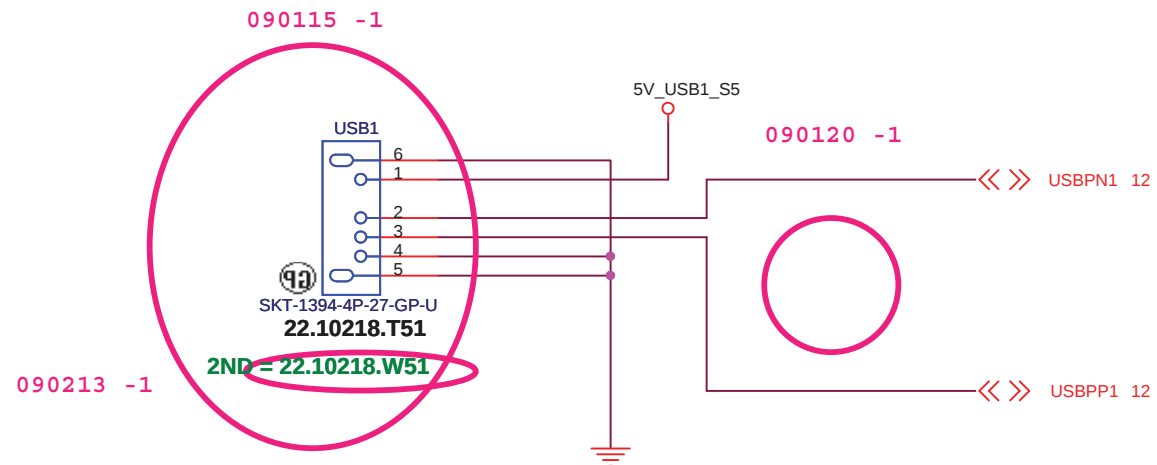
Date: Friday, March 06, 2009

Sheet 24 of 56

ODD Connector



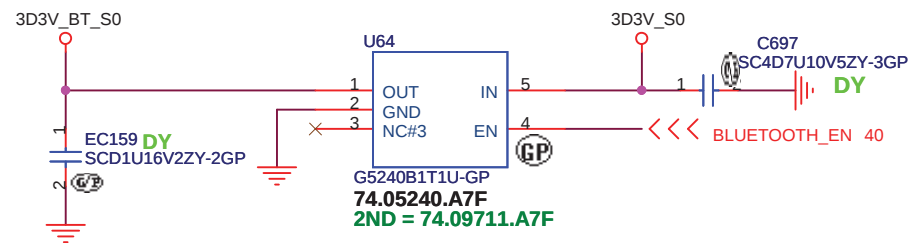
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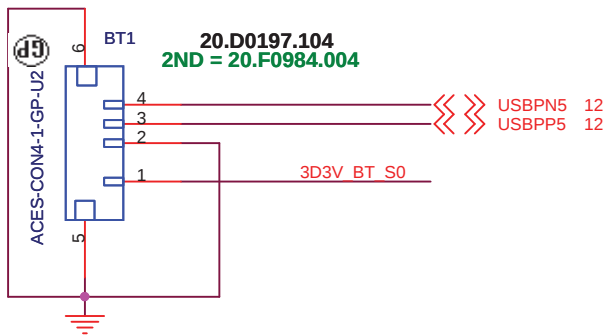
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Title		USB1	
Size	Document Number	Rev	
A4	JM70-PU	-2	
Date:	Friday, March 06, 2009	Sheet	26 of 56

BLUETOOTH MODULE

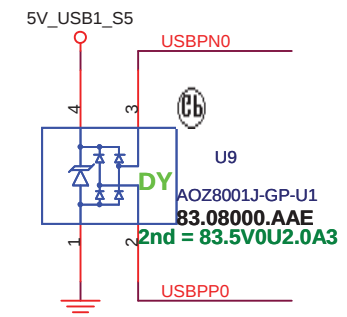
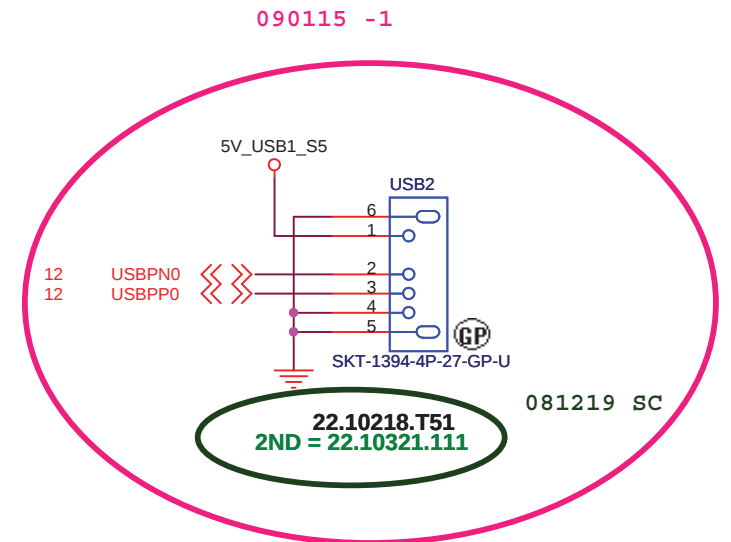


EC40 put near BLUE1 / all USB put one
choke near connector by EMI request



<Core Design>

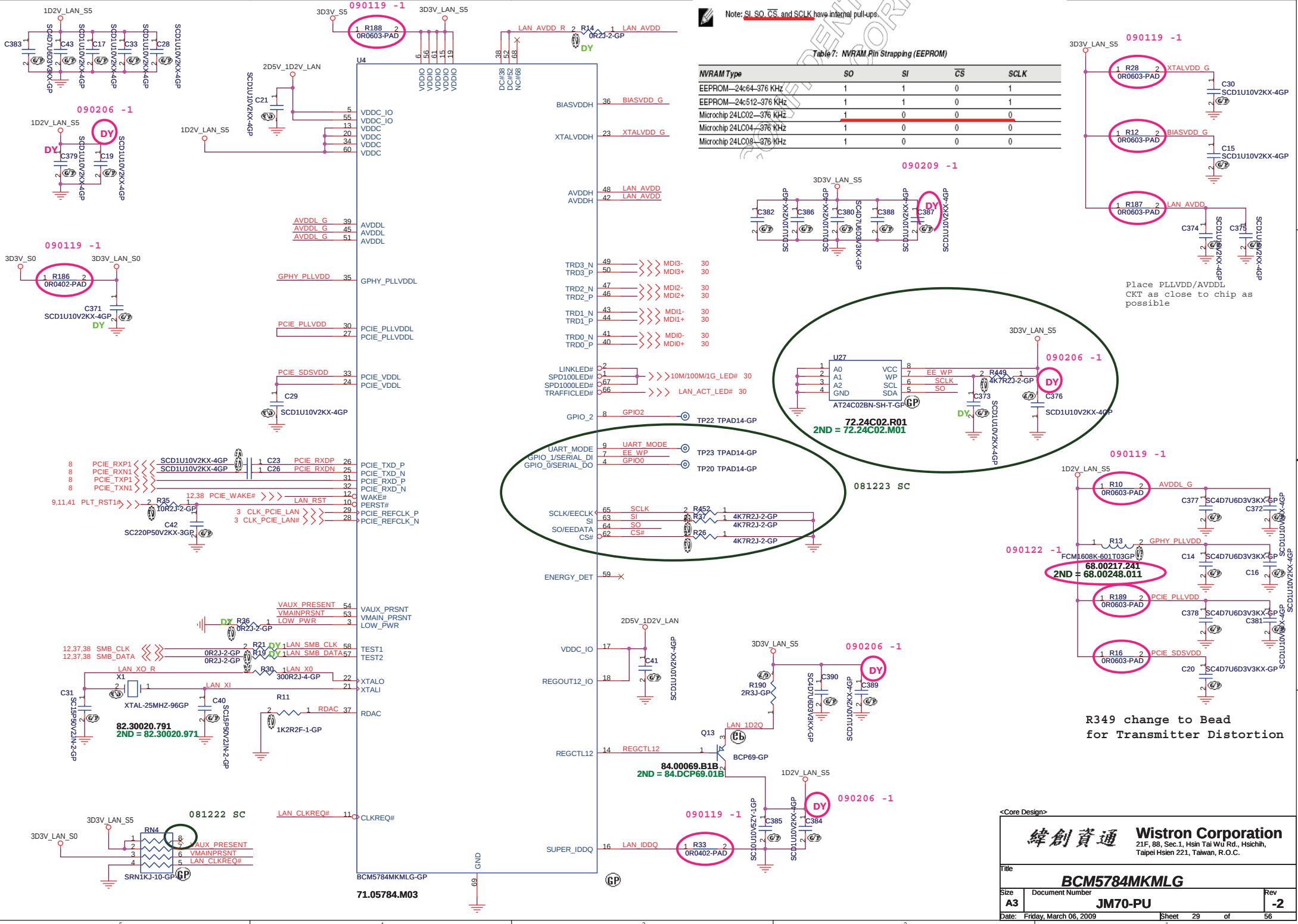
Title		Rev	
Size		Document Number	
Date:		Sheet	
Friday, March 06, 2009		27 of 56	
A4		JM70-PU	
-2			



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-2

Sheet 28 of 56



Note: SI, SO, CS, and SCLK have internal pull-ups.

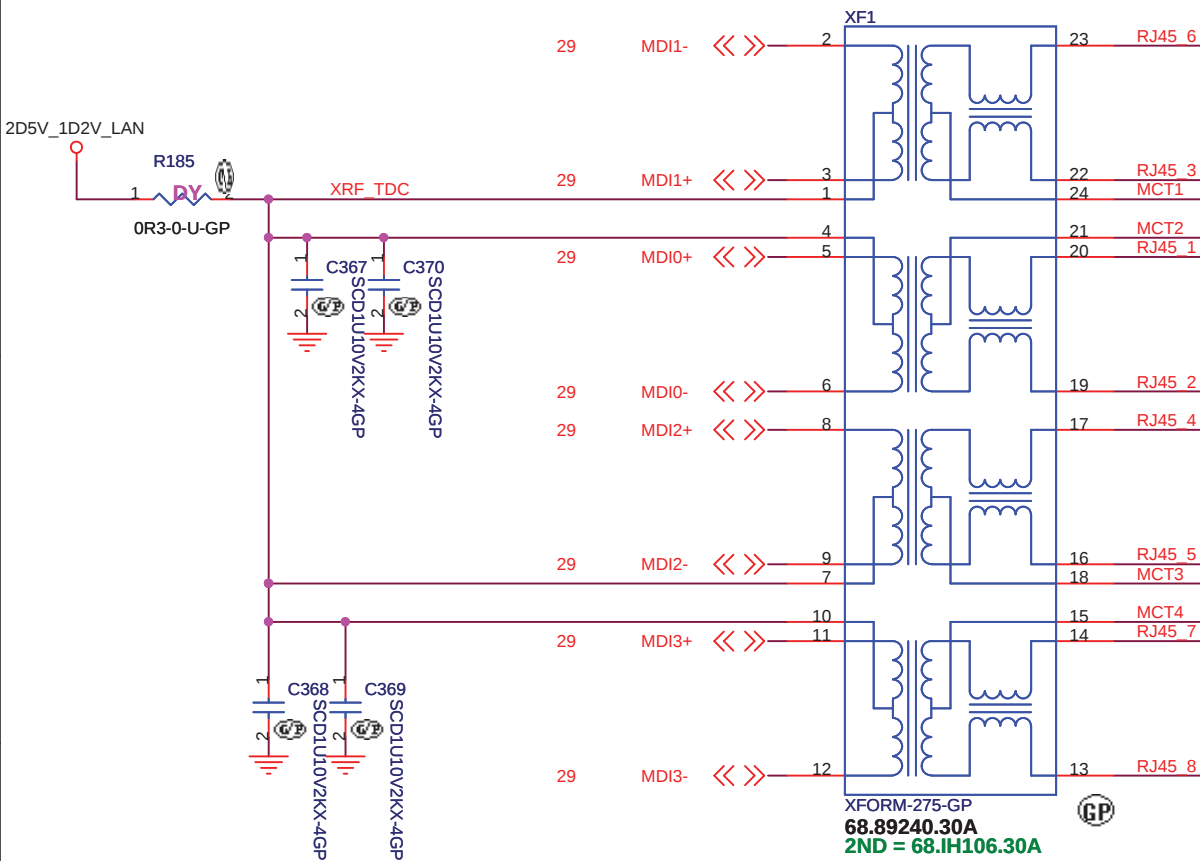
Table 7: NVRAM Pin Strapping (EEPROM)

NVRAM Type	SO	SI	CS	SCLK
EEPROM—24c64—376 KHz	1	1	0	1
EEPROM—24c512—376 KHz	1	1	0	1
Microchip 24LC02—376 KHz	1	0	0	0
Microchip 24LC04—376 KHz	1	0	0	0
Microchip 24LC08—376 KHz	1	0	0	0

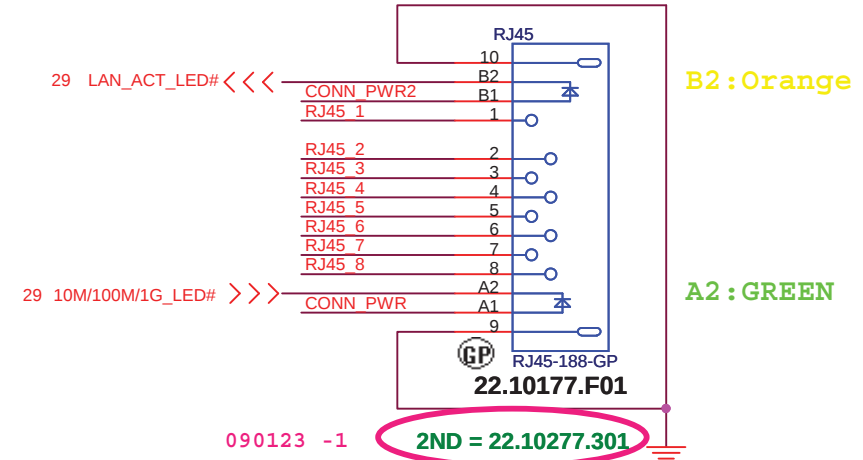
Place PLLVDD/AVDDL CKT as close to chip as possible

R349 change to Bead for Transmitter Distortion

LAN Connector

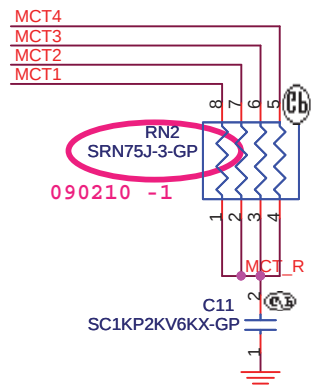


Soucrer want to add 3rd source 11/10
68.05009.301 GST5009-R LF
Angela Chi 0955-314886

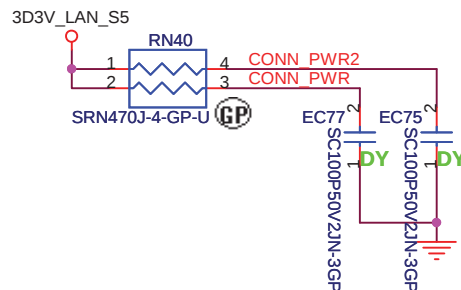


Green(A2), behavior is the
LAN Link: same for 10/100/1000 bits

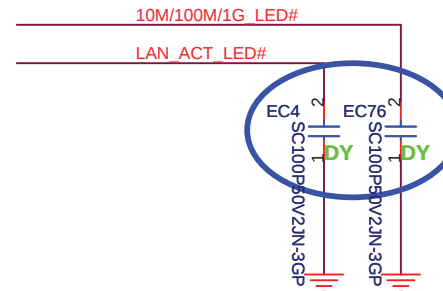
LAN Data: Yellow(B2), when LAN is
transferring data.



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



For EMI Near LAN1 CONN



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Title

LAN CONN

Size

A4

Document Number

JM70-PU

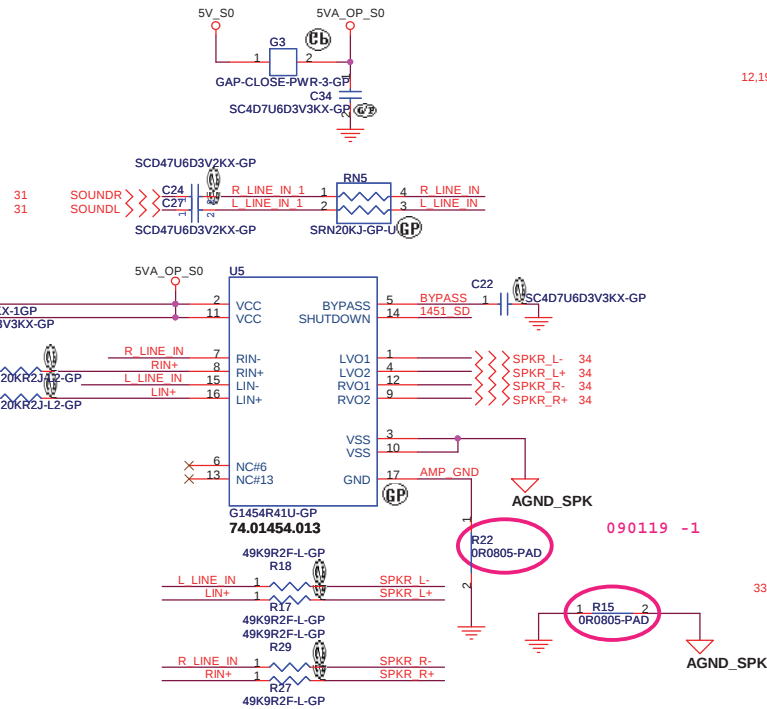
Rev

-2

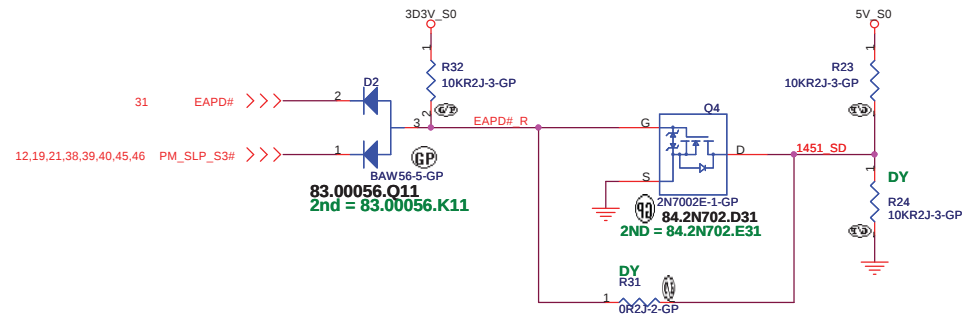
Date: Friday, March 06, 2009

Sheet 30 of 56

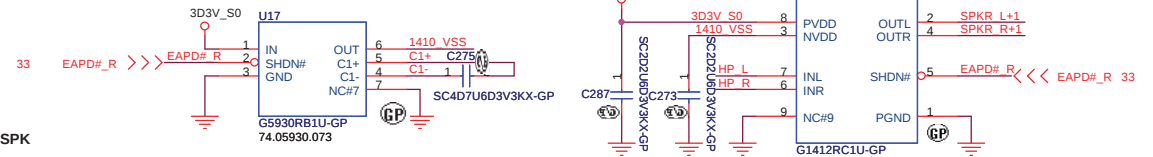
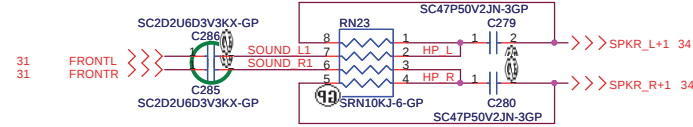
AUDIO OP AMPLIFIER



Gain= $R_f/R_i=49.9K/20K=2.495V/V$
 $f(HP)=1/(2 \pi * 20K * 0.47\mu f)=16.9Hz$
 If $V_{IN}=1.54V$ Gain=2.6V/V $R_L=4\Omega$ $V_O(peak)=4V$
 $V(rms)=2.828V$
 Power= $2.828^2/4=1.999W$



090101 SC

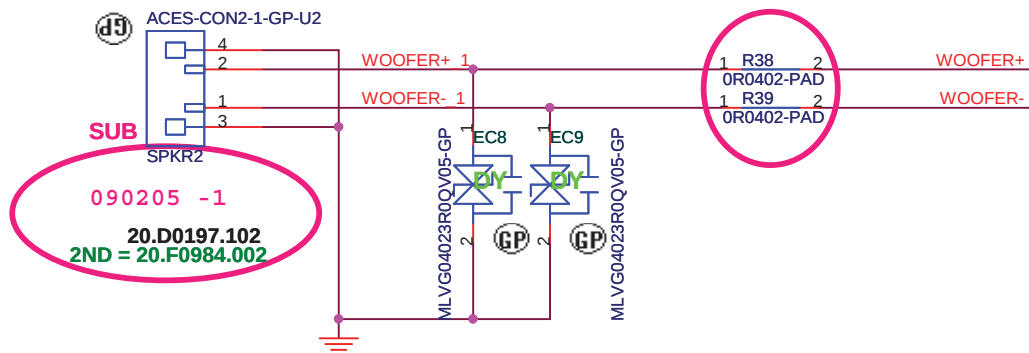
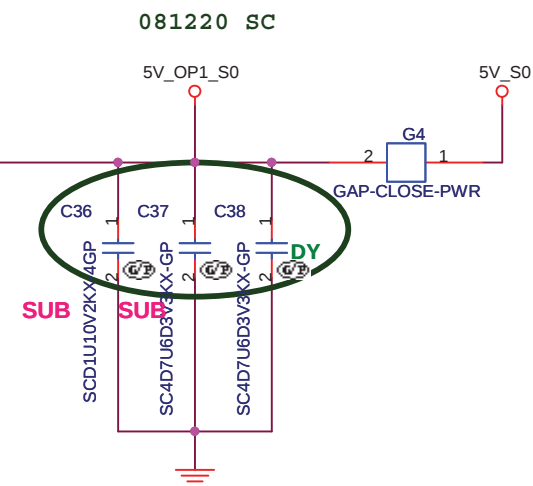
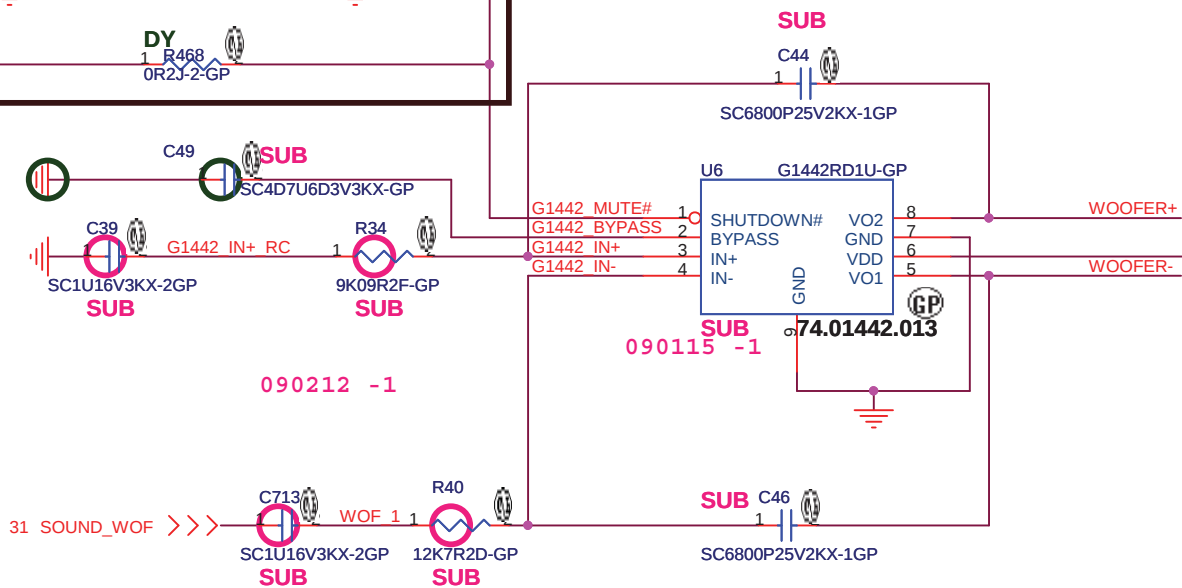
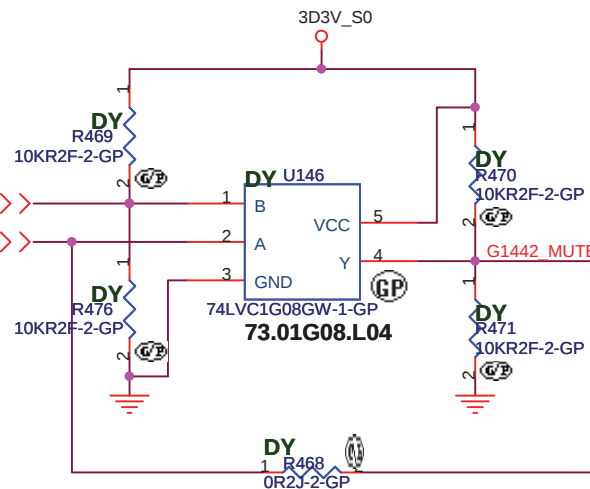


Gain= $R_f/R_i=20K/18K=0.9V/V$
 $f(HP)=1/(2 \pi * 20K * 0.47\mu f)=16.9Hz$
 If $V_{IN}=1.54V$ Gain=0.9V/V $R_L=4\Omega$ $V_O(peak)=4V$ $V(rms)=2.828V$
 Power= ?

<Core Design>

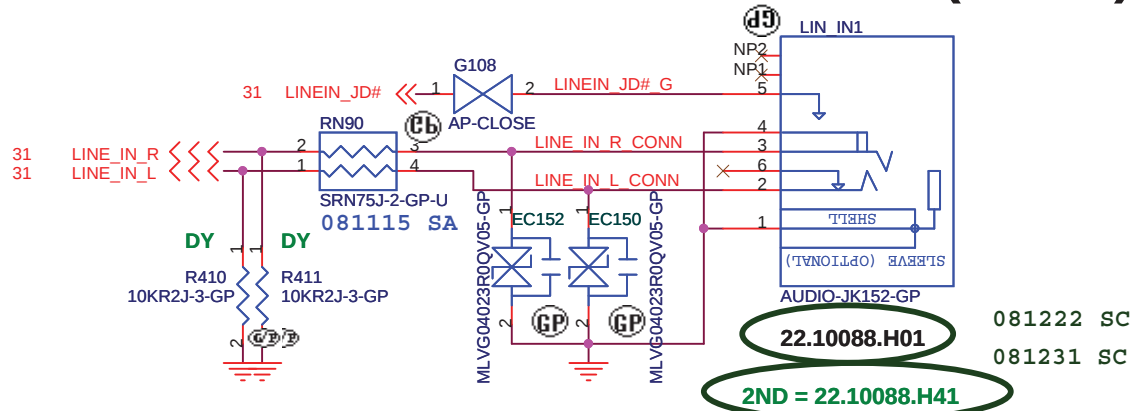
緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title			AUDIO AMP
Size	Document Number	Rev	
A3	JM70-PU	-2	
Date:	Friday, March 06, 2009	Sheet	32 of 56

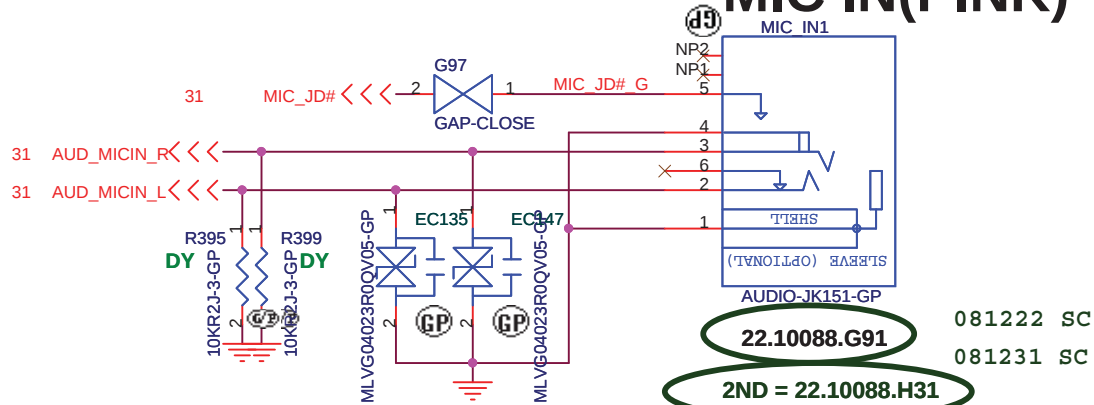


Sheet 33 of 56

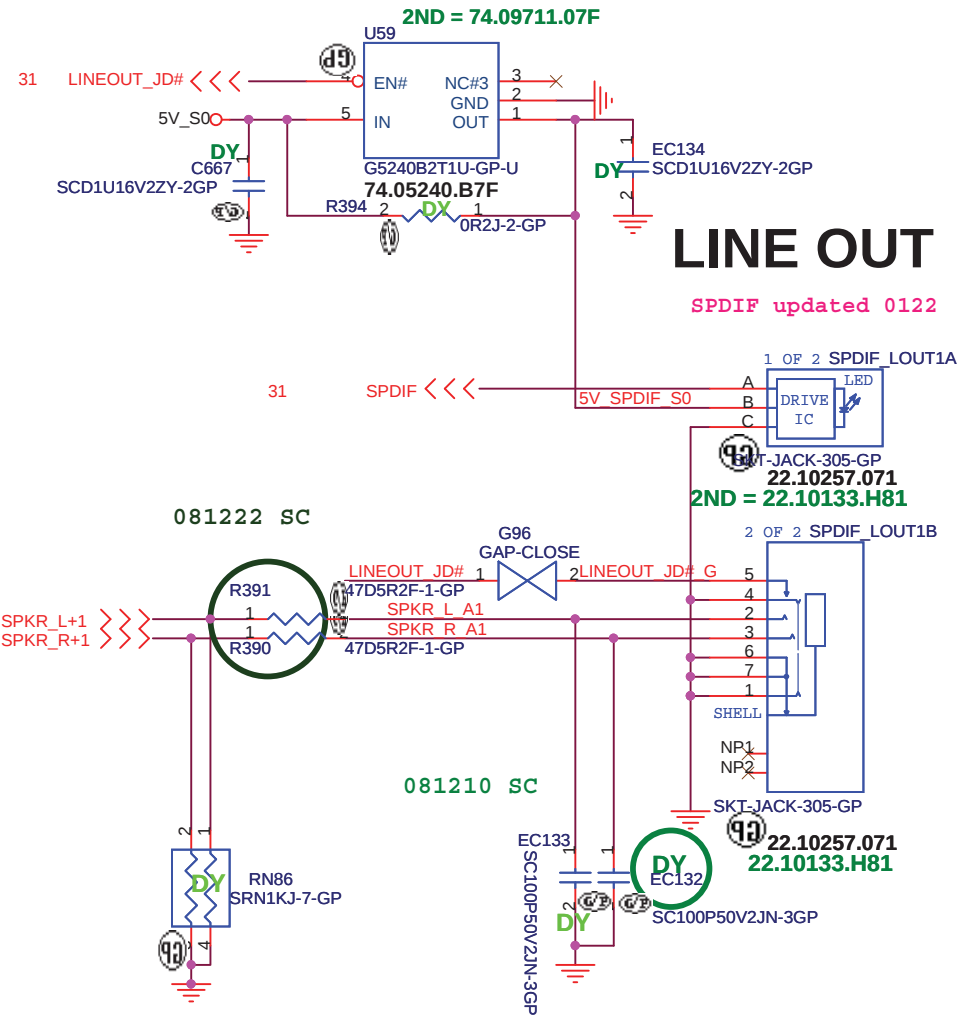
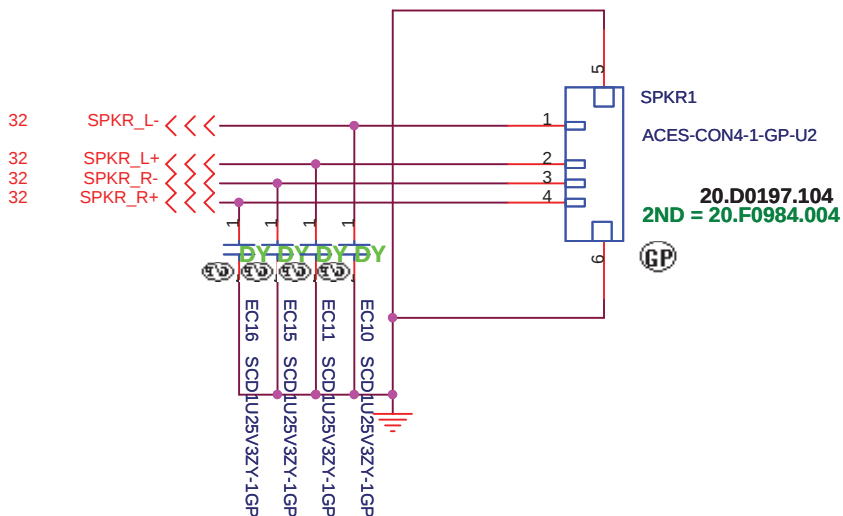
LINE IN(BLUE)



MIC IN(PINK)



REAR Speaker



<Core Design>

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Title

AUDIO JACK

Size
A4

Document Number

JM70-PU

Rev
-2

Date: Friday, March 06, 2009

Sheet 34 of 56

[illegible]

Pin Label	Pin Number	Component Pin
ACZ_SDATAOUT_MDC	C362	1
ACZ_SYNC	C361	dy
ACZ_RST#	C363	dy
ACZ_BCLK_MDC	C365	1

Sheet 35 of 56

090119 -1



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Title

Mini Card

Size
A

	Document Number
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JM70-PU

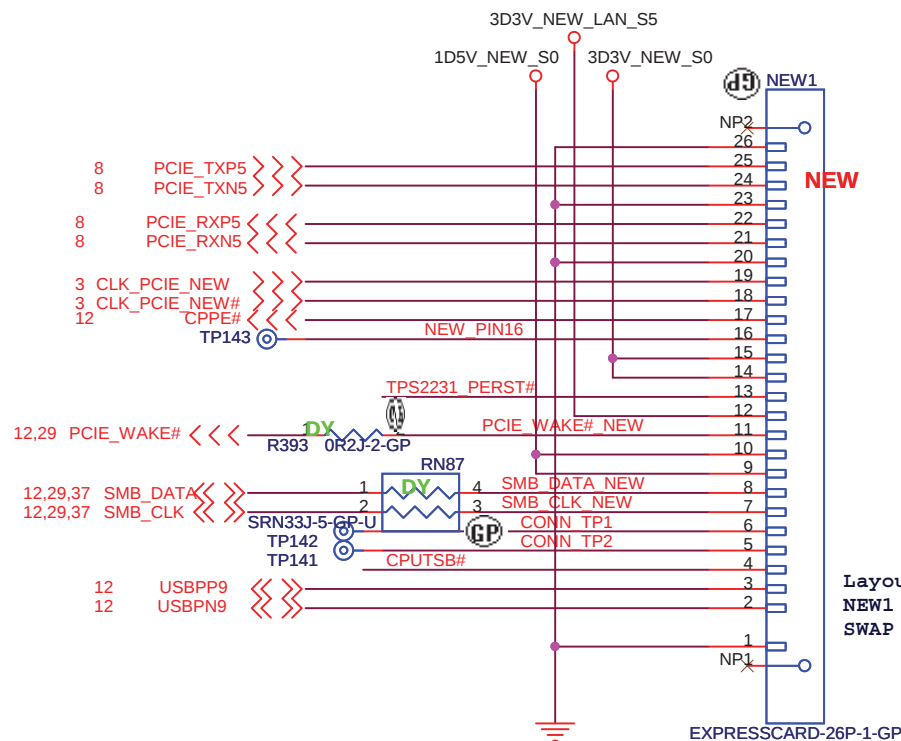
Date: Friday, March 06, 2009

Sheet 37 of 56

-2

NEWCARD Connector

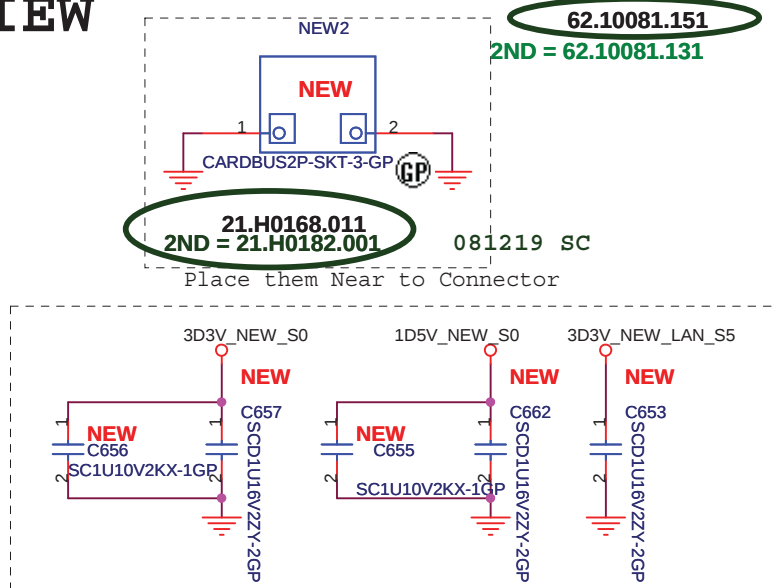
ENG stage without NEW card function 12/22



Layout Request 1226
NEW1 & NEW2
SWAP 1st & 2nd

TOP VIEW

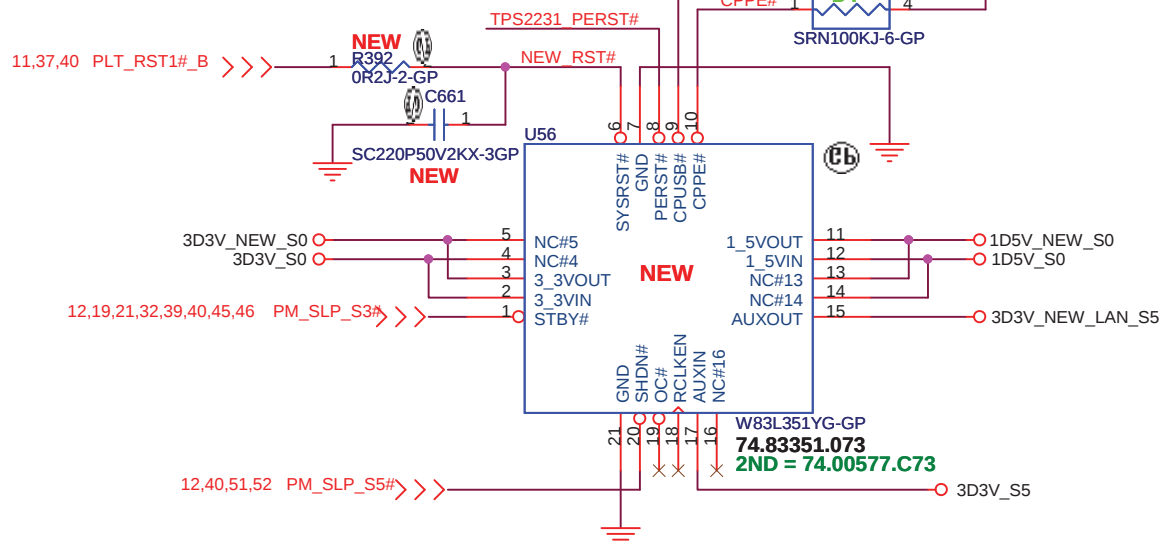
1
26



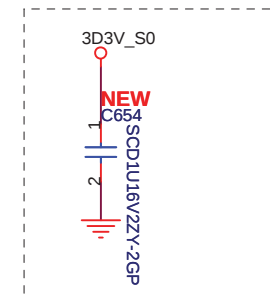
081219 SC

62.10081.151
2ND = 62.10081.131

21.H0168.011
2ND = 21.H0182.001
081219 SC



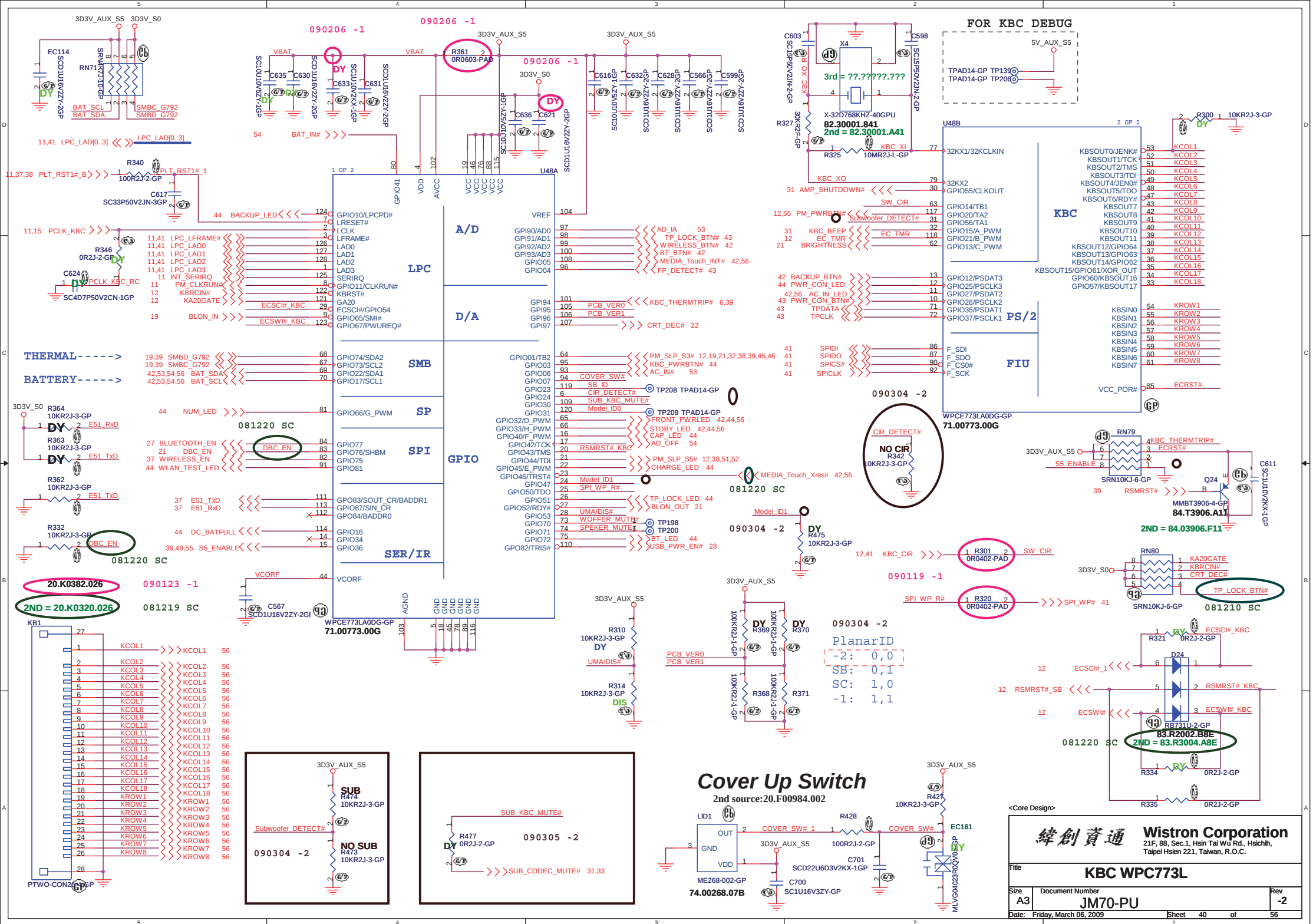
Place them Near to Chip



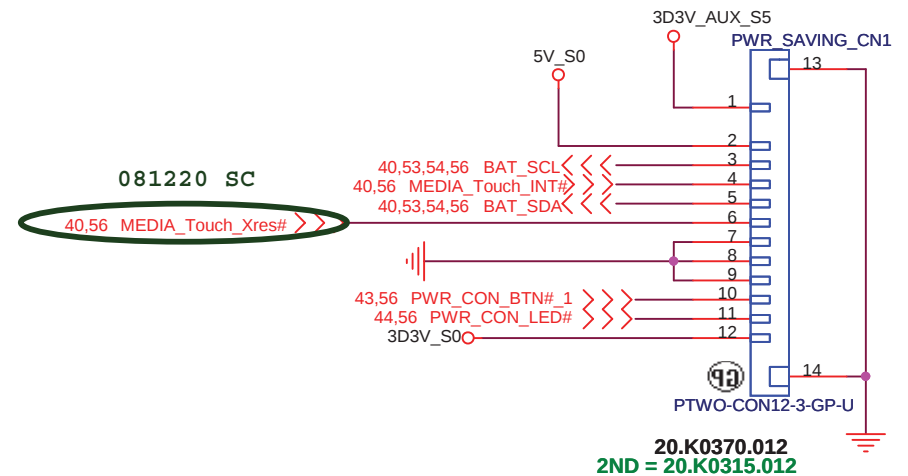
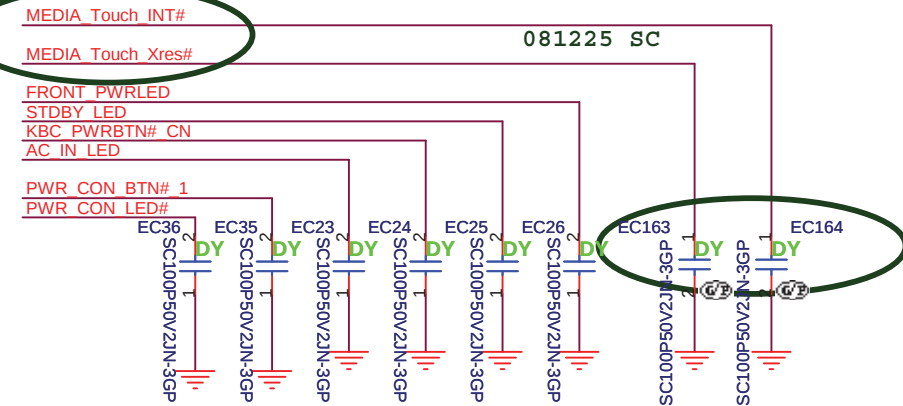
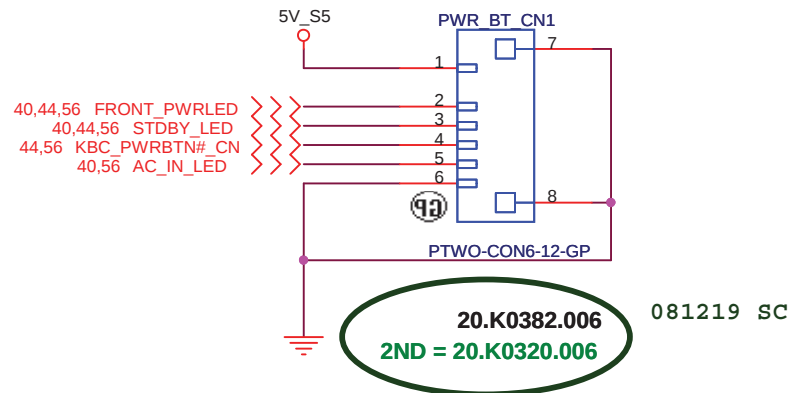
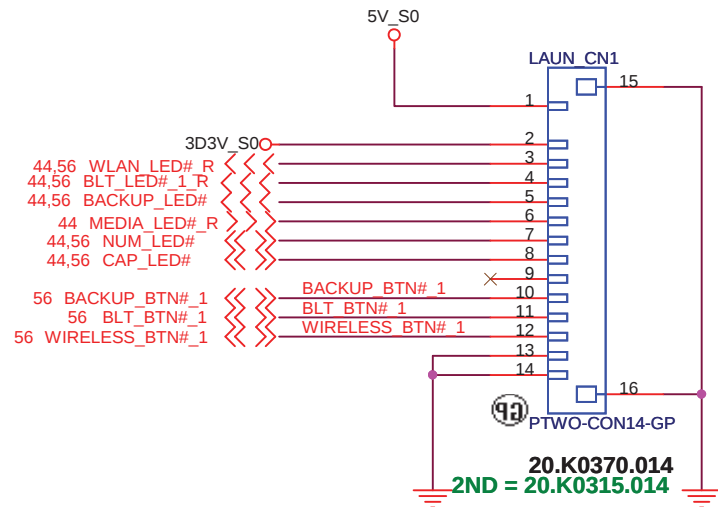
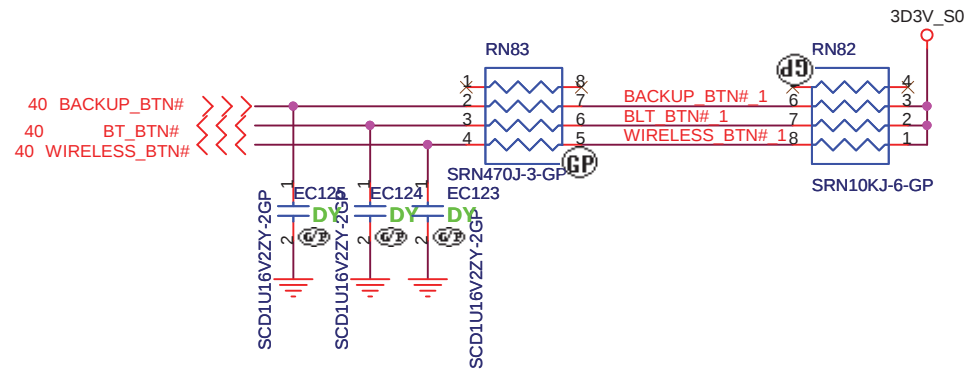
74.00577.C73
new card power switch
GMT cost down solution

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Title		
NEW CARD		
Size	Document Number	Rev
A4	JM70-PU	-2
Date	Friday, March 06, 2009	Sheet 38 of 56



LAUNCH



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Title

LAUNCH & LID

Size
A4

Document Number

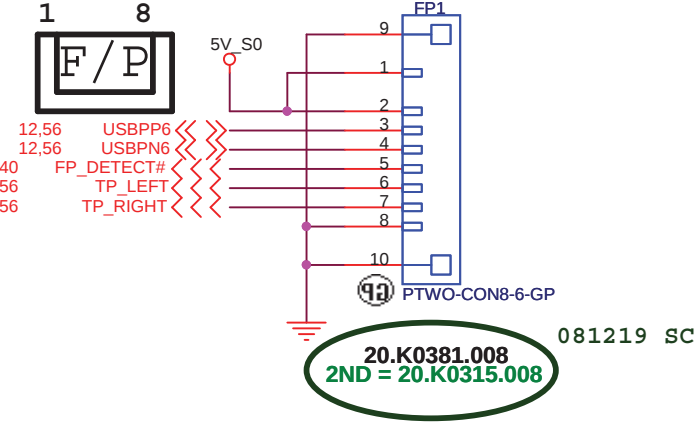
JM70-PU

Rev
-2

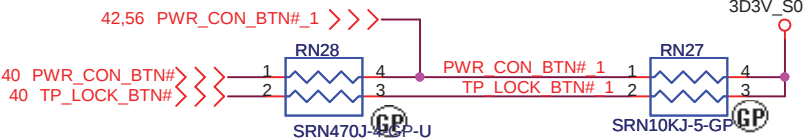
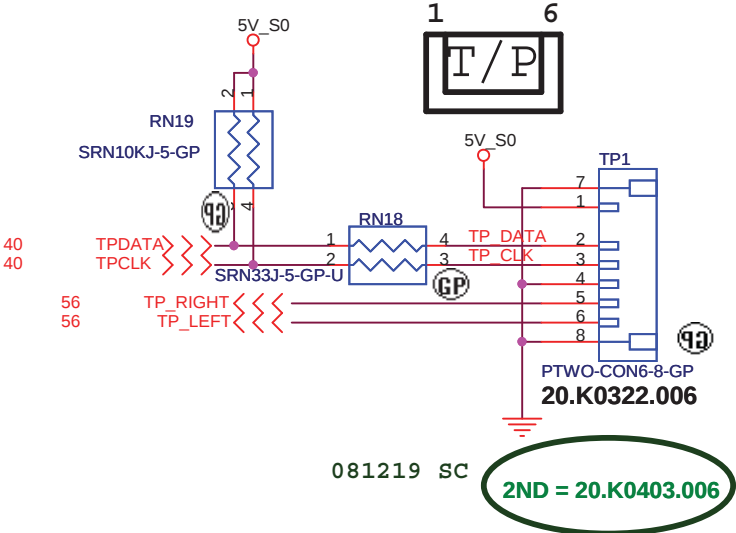
Date: Friday, March 06, 2009

Sheet 42 of 56

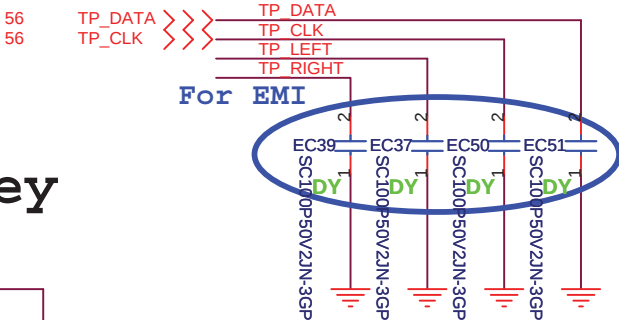
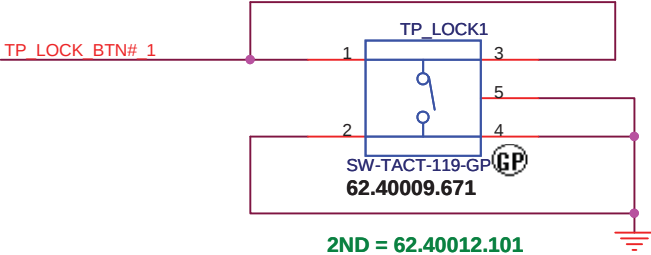
Finger printer



TOUCH PAD



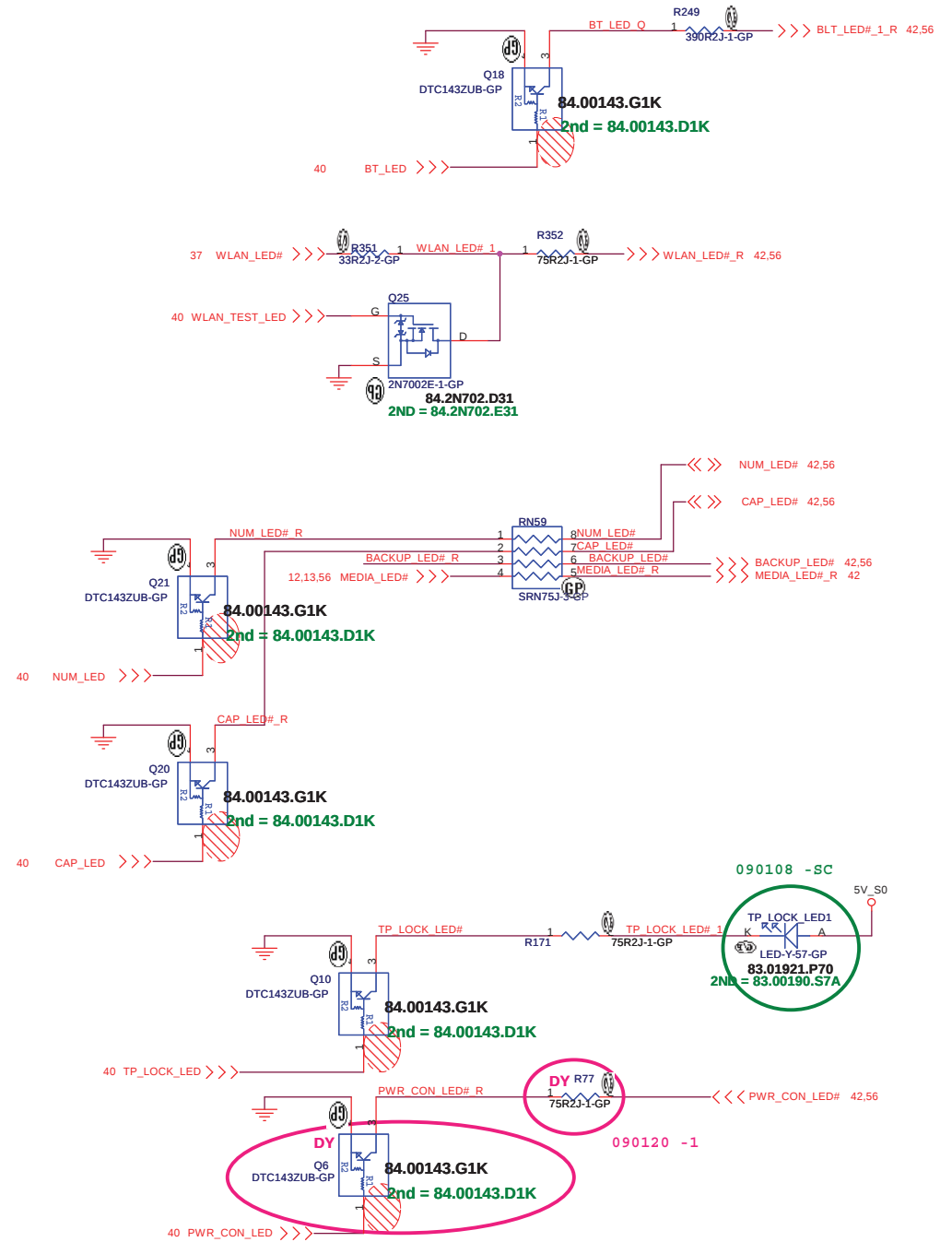
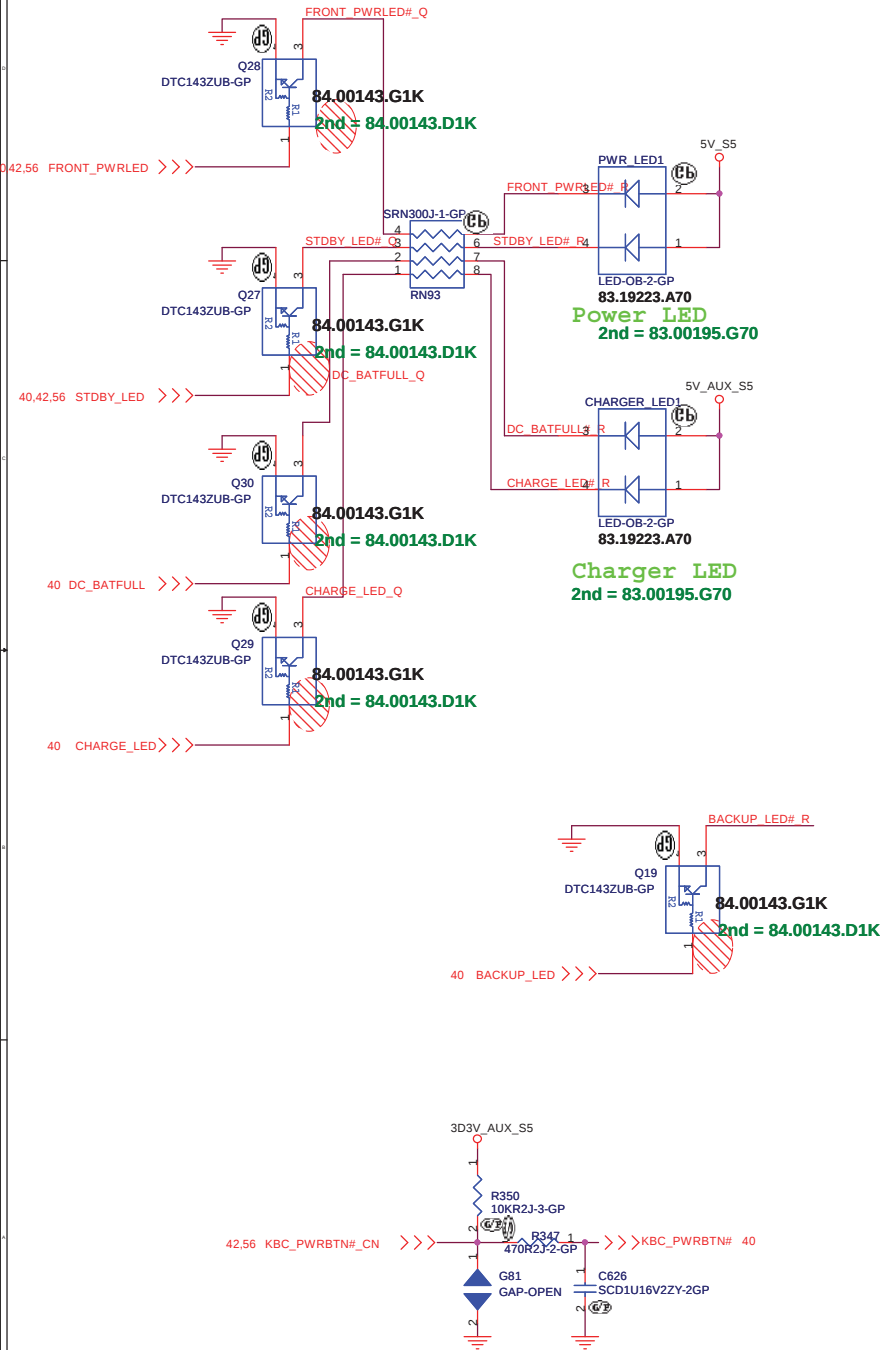
TP_LOCK key

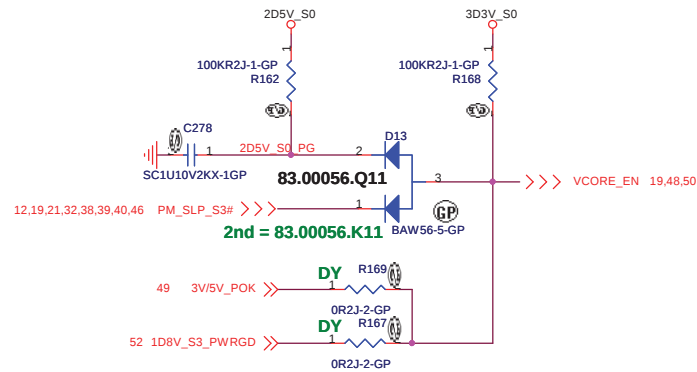


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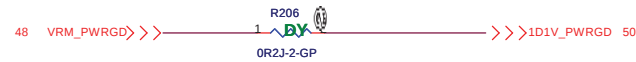
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Title		
Finger Printer		
Size	Document Number	Rev
A4	JM70-PU	-2
Date:	Friday, March 06, 2009	Sheet 43 of 56

LED

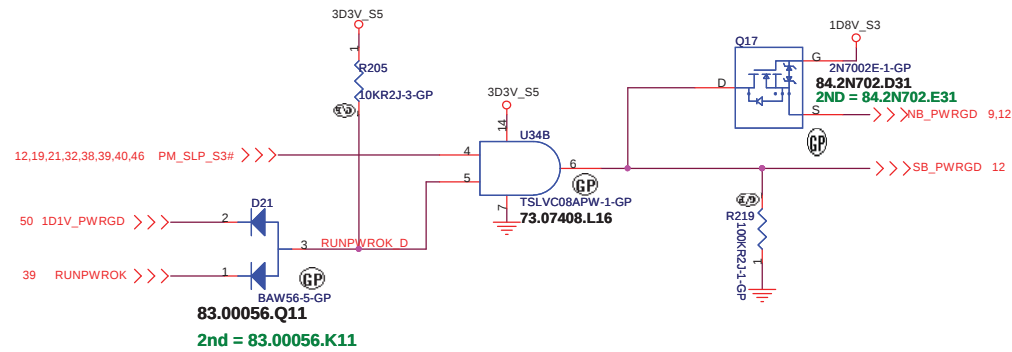




P/H @ 1D8V_S3 PAGE



Reference schematic recommend



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Title

POWER ON LOGIC

Size
A3

Document Number

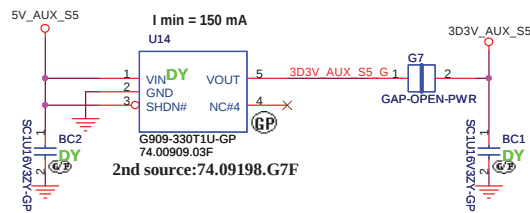
JM70-PU

Date: Friday, March 06, 2009

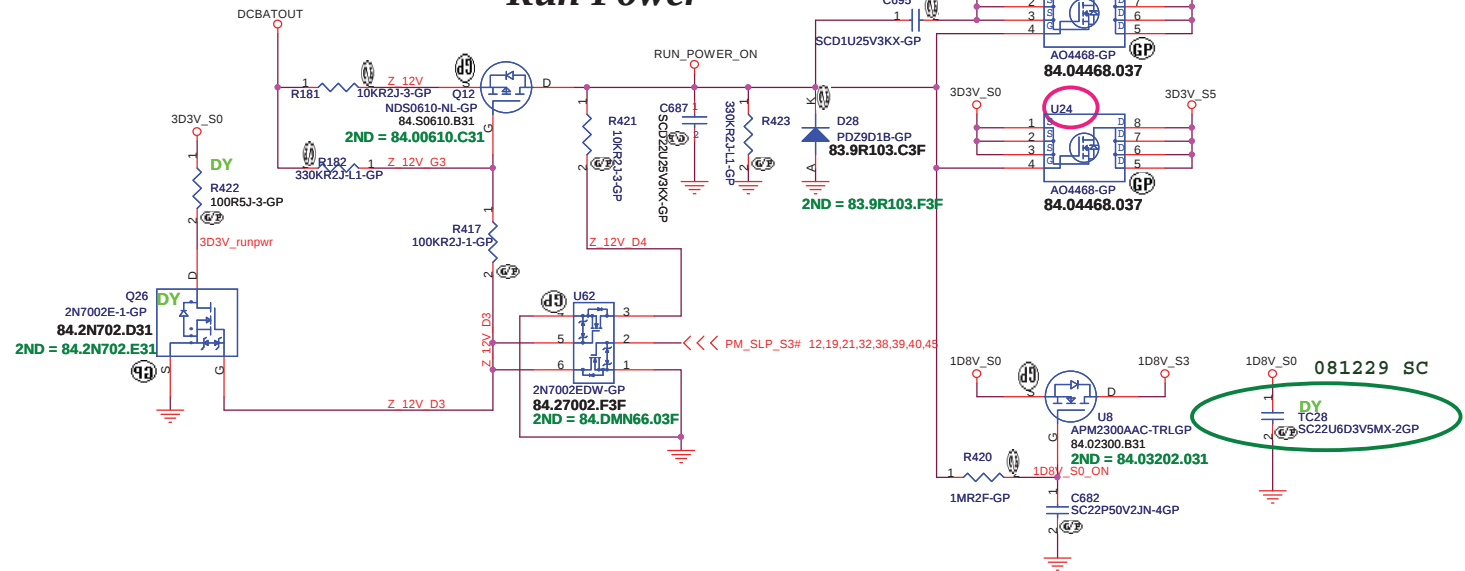
Sheet 45 of 56

Rev
-2

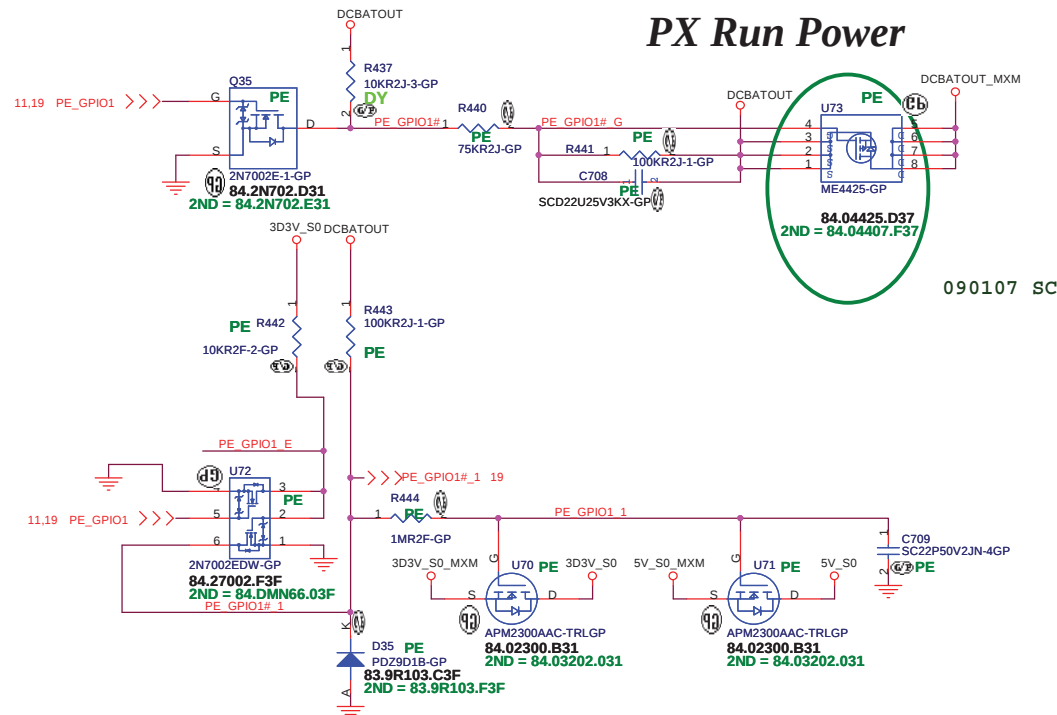
Aux Power 3D3V_AUX_S5



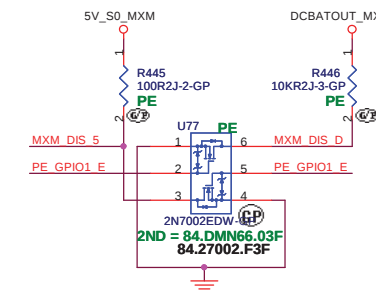
Run Power



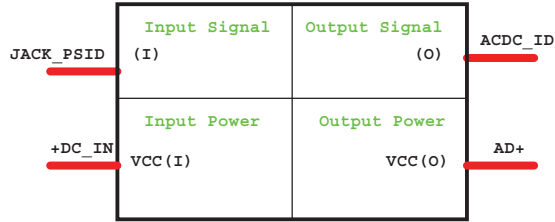
PX Run Power



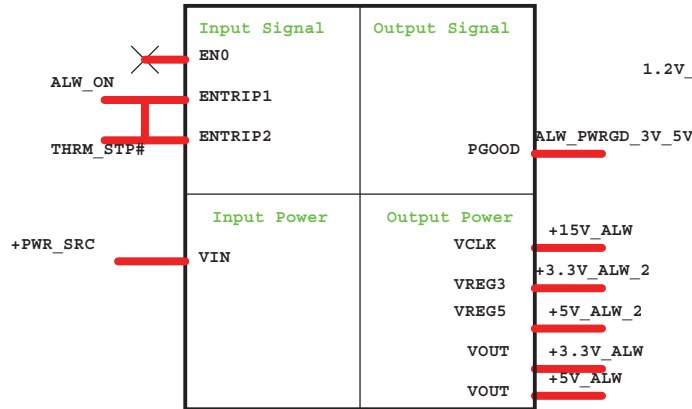
PX Run Power Discharge circuit



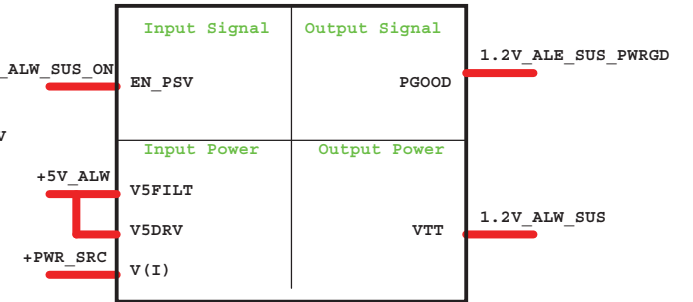
Adapter



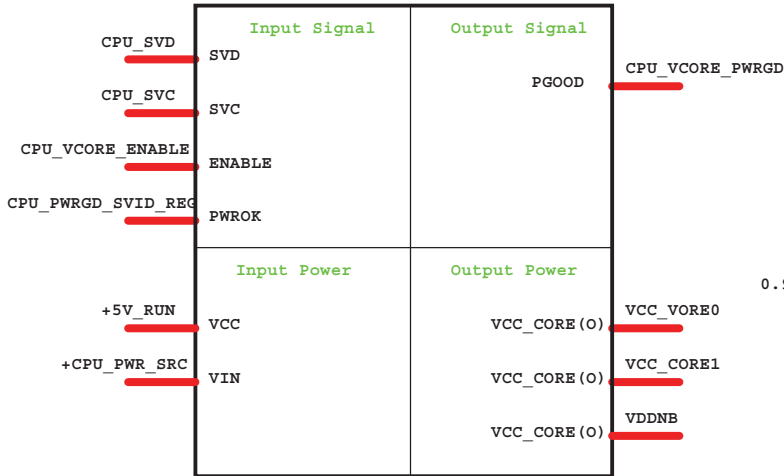
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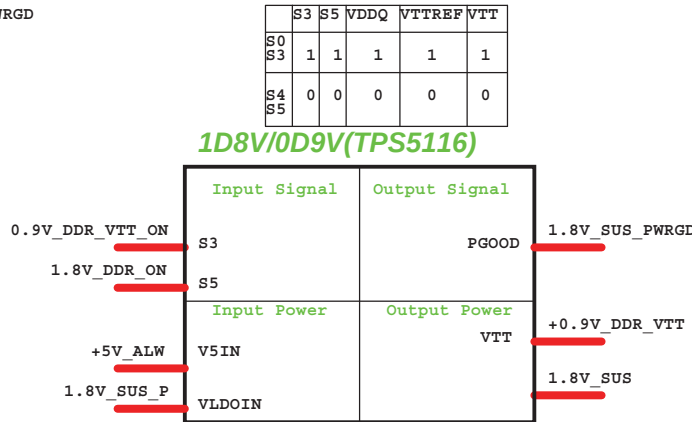
DCDC 1D2V(TPS5117)



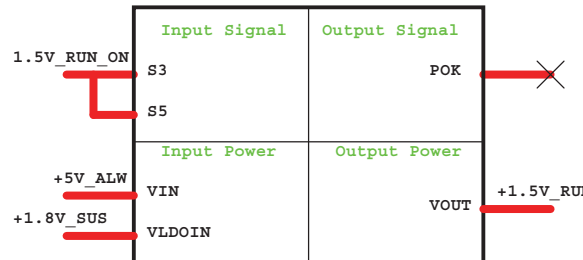
CPU_CORE ISL6265HRTZ



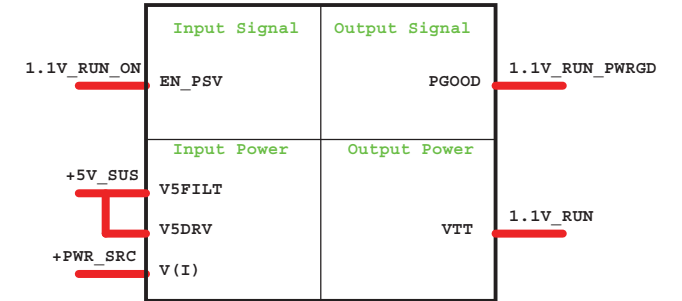
1D8V/0D9V(TPS5116)



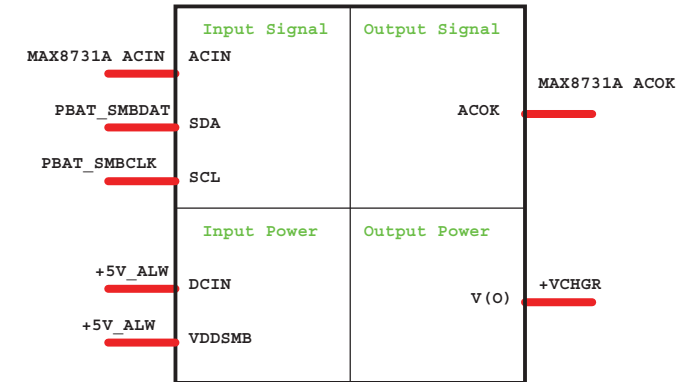
1.5V_LDO



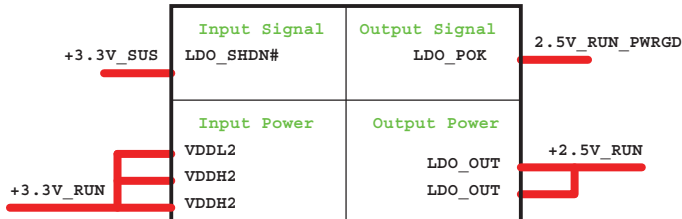
1D1V(TPS5117)



CHARGER BQ24745



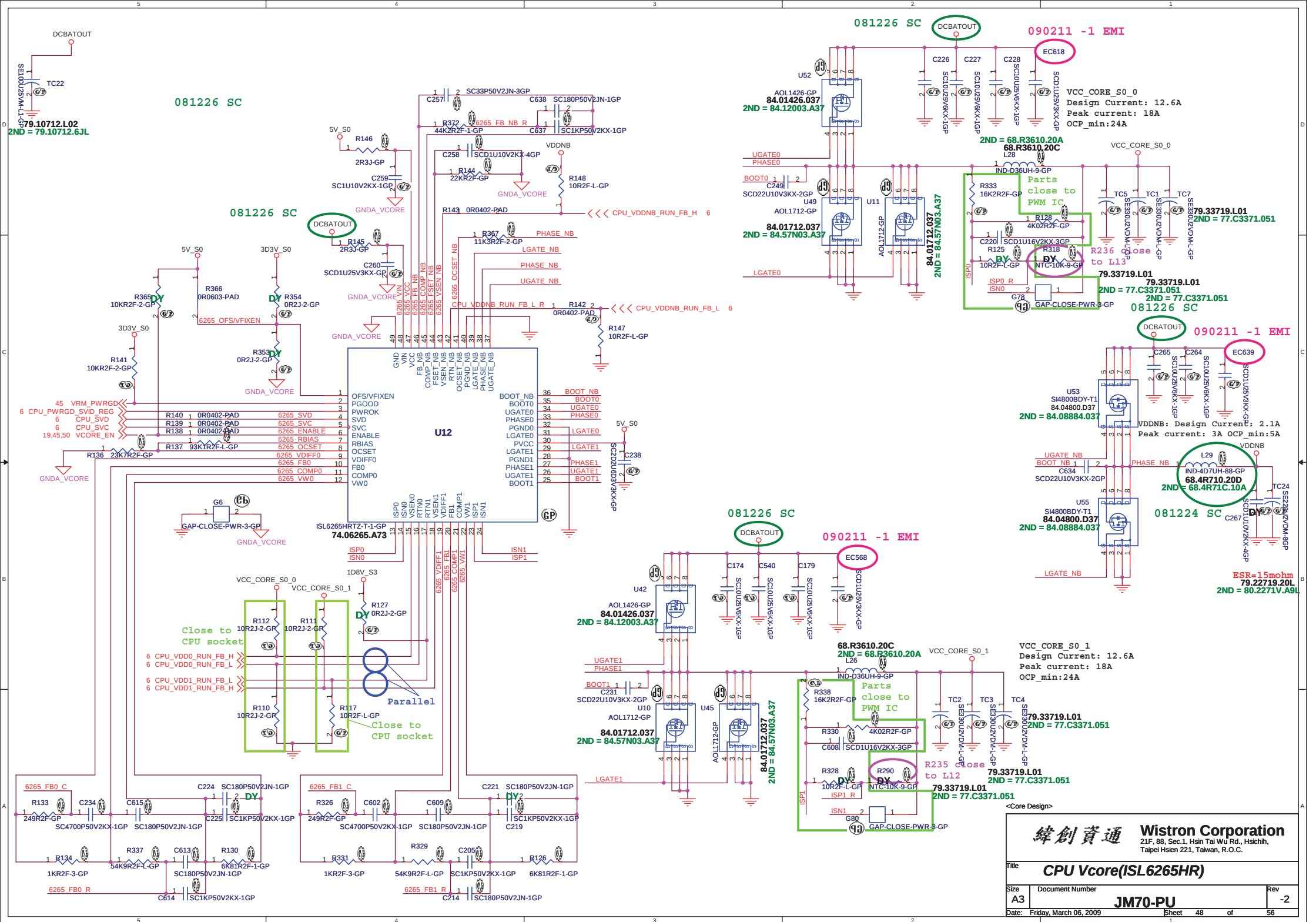
2.5V LDO EMC4002

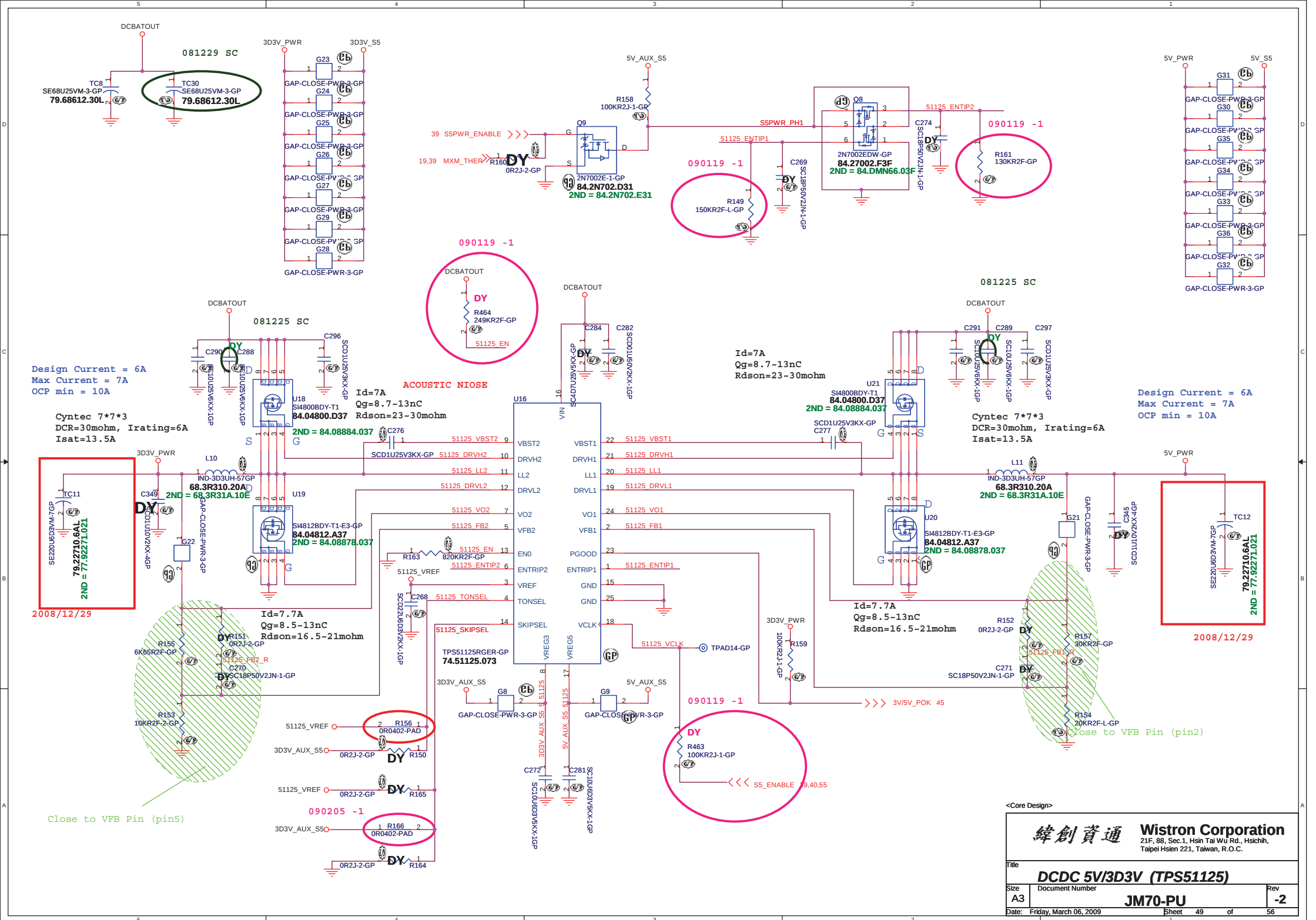


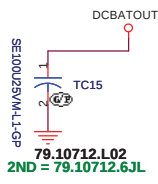
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Title Power Block Diagram		
Size A3	Document Number JM70-PU	Rev -2
Date: Monday, March 02, 2009	Sheet 47 of 56	



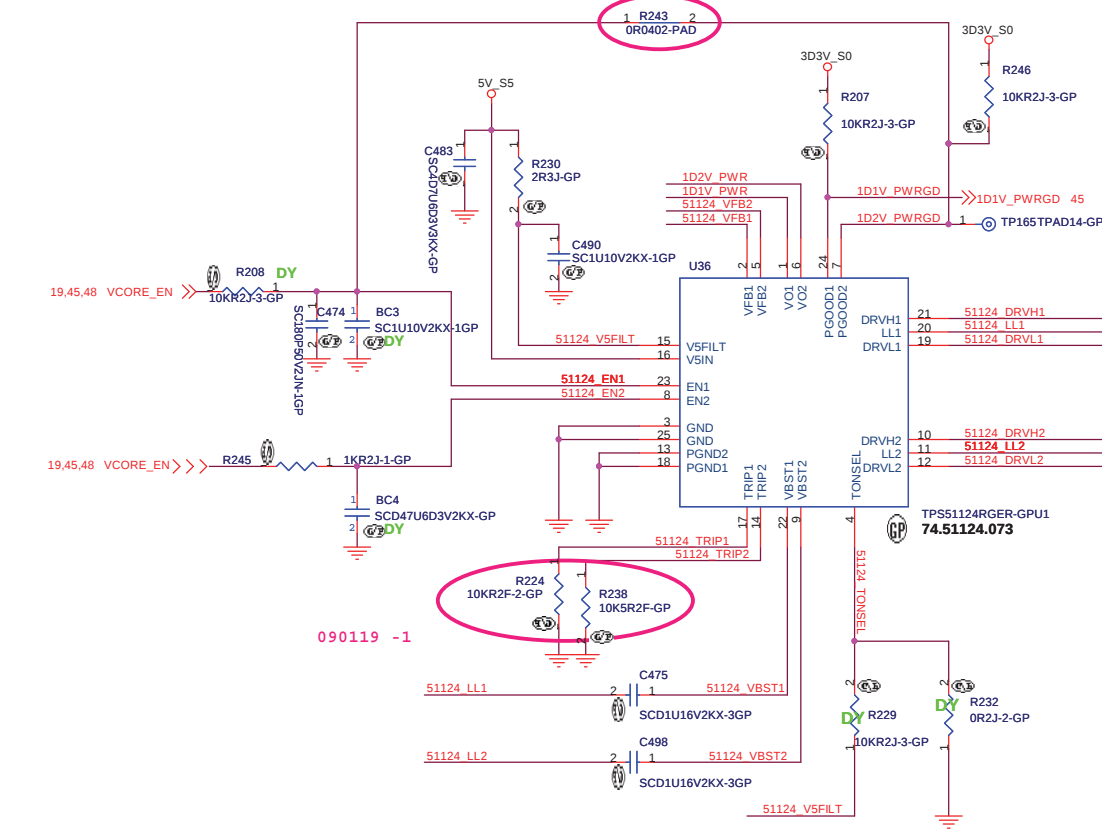




$$V_{trip} (mV) = R_{trip} (Kohm) * 10 (uA)$$

$$I_{ocp} = (V_{trip} / R_{dson}) + ((1 / (2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$$

090205 -1

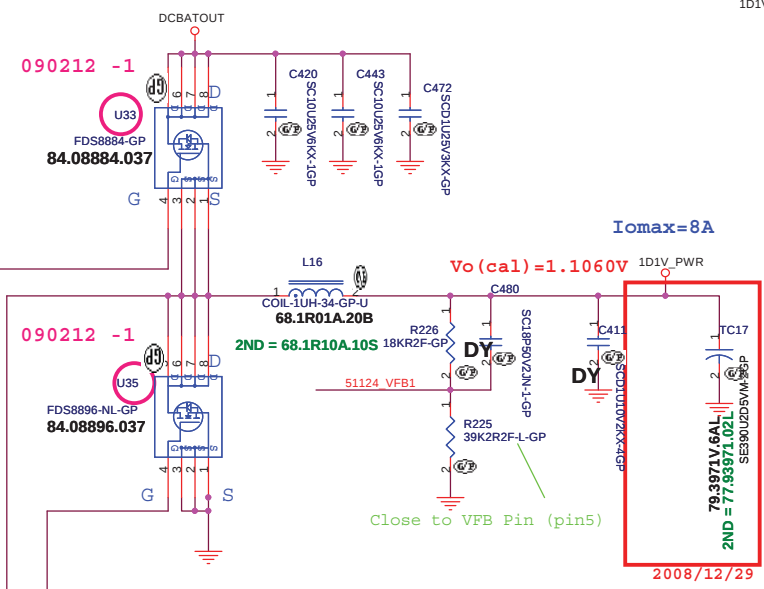


090119 -1

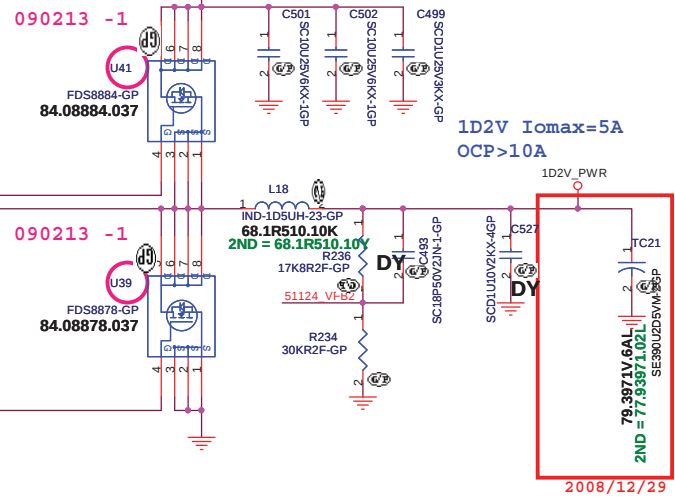
	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$$V_{out} = 0.758V * (R1 + R2) / R2 \text{ --- PWM mode}$$

$$V_{out} = 0.764V * (R1 + R2) / R2 \text{ --- Skip Mode}$$



20080307_Modify by
Brian
ACOUSTIC NIOSE



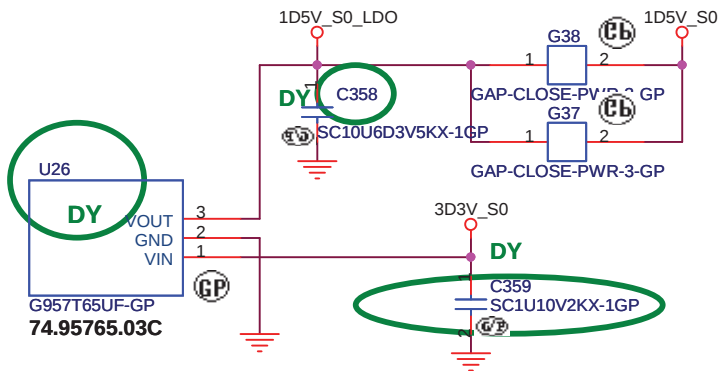
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Title			TPS51124 1D1V 1D2V	
Size	Document Number		Rev	
A3	JM70-PU		-2	
Date:	Friday, March 06, 2009	Sheet	50	of 56

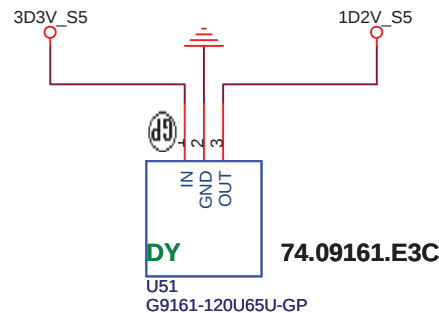
G957

1D5V_S0
Iomax=1A

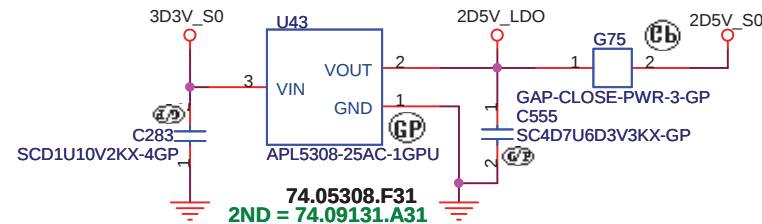


081230 SC

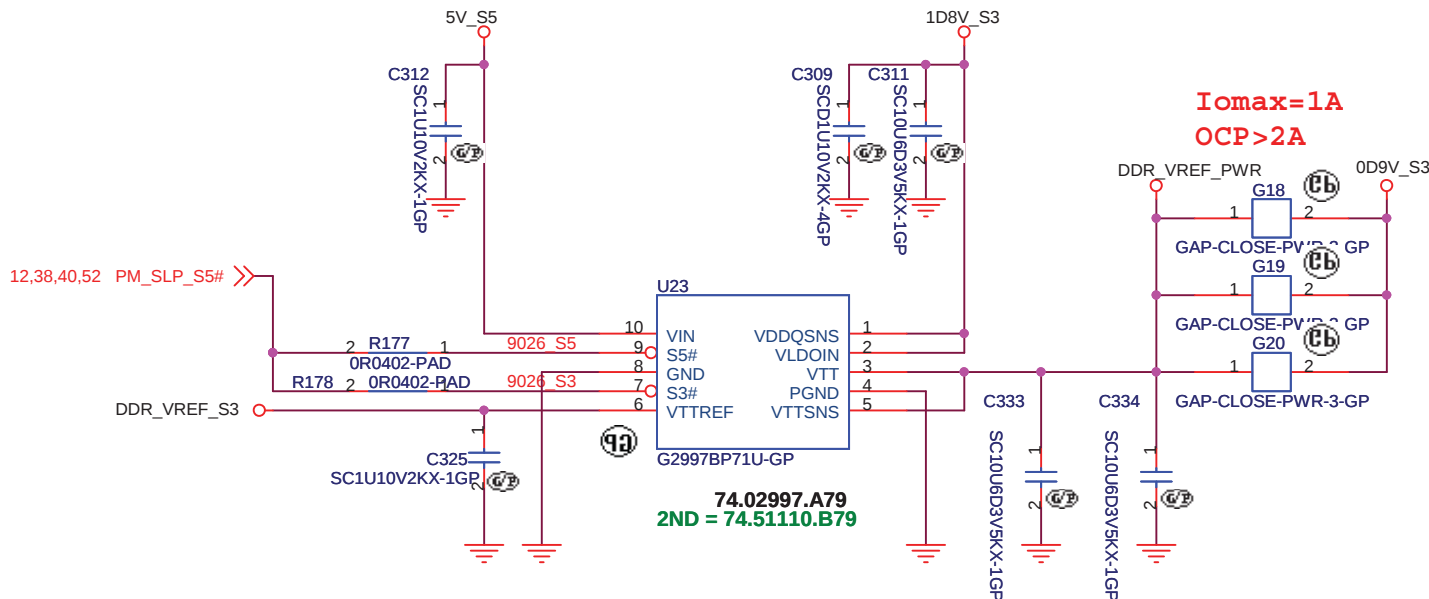
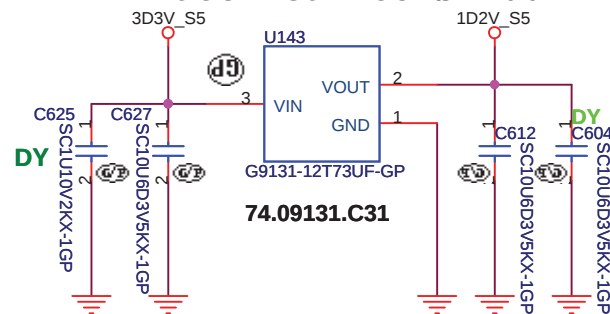
1D2V_S5
Iomax=400mA



2D5V_S0
Iomax=0.3A 2D5V/300mA



Place near to SB700



Iomax=1A
OCP>2A

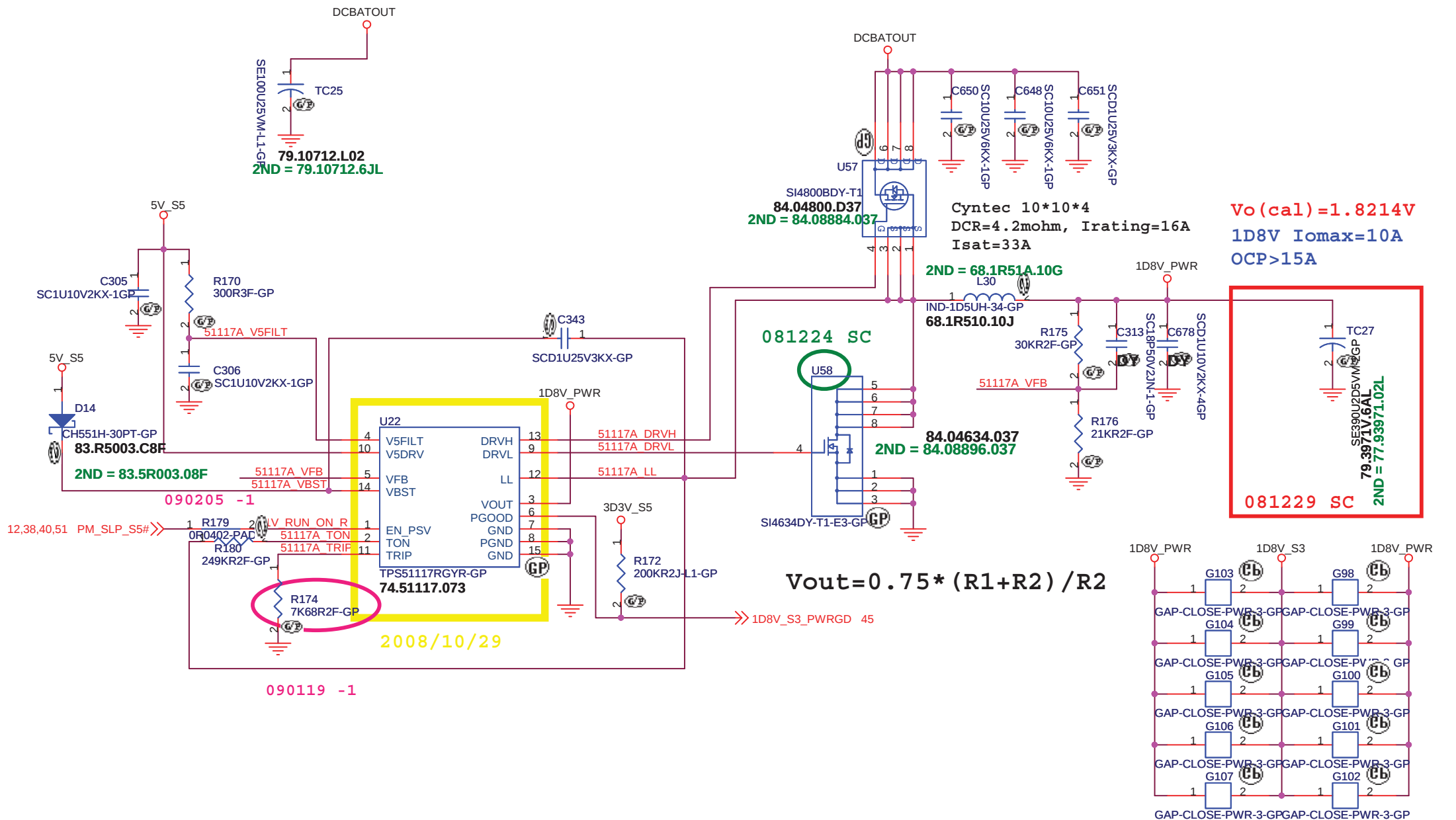
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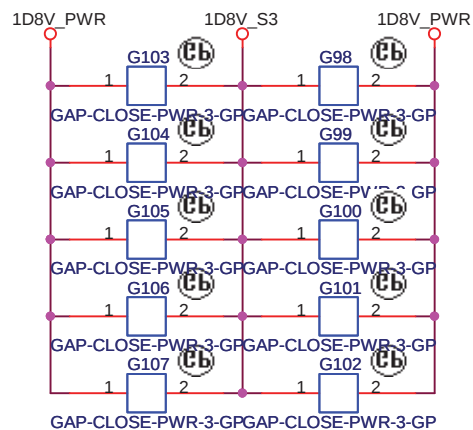
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
0D9V&2D5V&1D25V&1D5V		
Size	Document Number	Rev
A4	JM70-PU	-2
Date	Friday, March 06, 2009	Sheet 51 of 56



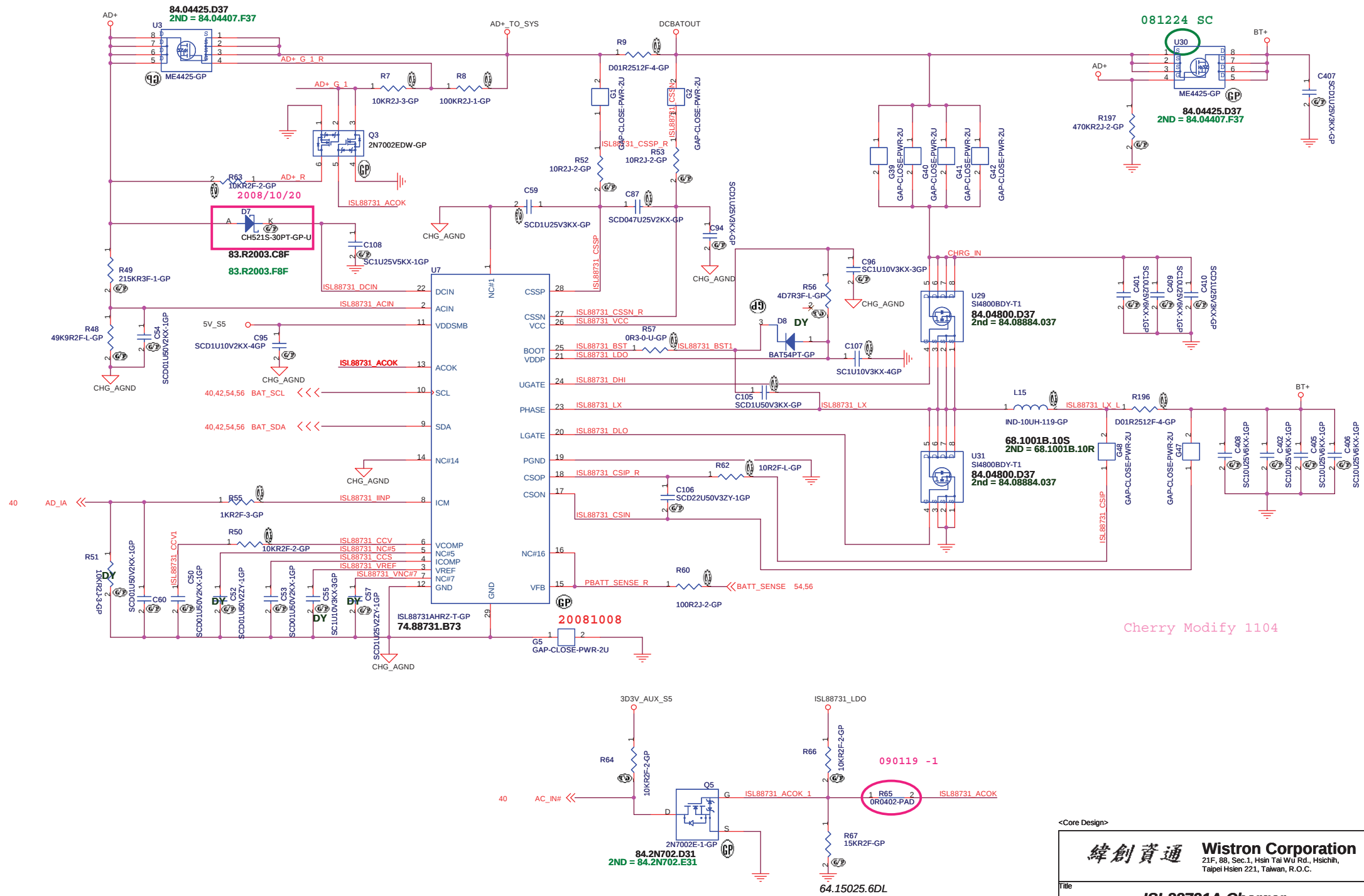
Vo(cal)=1.8214V
1D8V Iomax=10A
OCP>15A

$$V_{out} = 0.75 * (R1 + R2) / R2$$



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Title			
1D8V(TPS5117)			
Size	Document Number		Rev
A4	JM70-PU		-2
Date:	Friday, March 06, 2009	Sheet 52 of	56



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Title			ISL88731A Charger	
Size	Document Number			Rev
A3		JM70-PU		-2
Date:	Friday, March 06, 2009	Sheet	53	of 56



